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LIST OF ABBREVIATIONS

NPC	*Neutral Point Clamped*
FCMC	*Flying Capacitor Multilevel Converter*
DC	*Direct Current*
FC	*Flying Capacitor*
CHB	*Cascaded H-Bridge*
MMC	*Modular Multilevel Converter*
HVDC	*High Voltage Direct Current*
AC	*Alternating Current*
NNPC	*Nested Neutral Point Clamped*
PUC	*Paced U-Cell*
MLDLCI	*Multilevel DC Link Inverter*
SSPS	*Switched Series Parallel Sources*
ICEs	*Internal Combustion Engines*
HEV	*Hybrid Electric Vehicle*
MG	*Motor / Generator*
SOC	*State of charge*
PV	*Photo Voltaic*
SPWM	*Sinusoidal Pulse Width Modulation*
SVPWM	*Space Vector Pulse Width Modulation*
LS-PWM	*Level Shifted Pulse Width Modulation*
PWM	*Pulse Width Modulation*
PD	*Phase Disposition*
POD	*Phase Opposition Disposition*
APOD	*Alternate Phase Opposition Disposition*
PS-PWM	*Phase Shifted Pulse Width Modulation*
PD-PWM	*Phase Disposition Pulse Width Modulation*

PSD-PWM *Phase Shifted Disposition Pulse Width Modulation*

COD-PWM *Carrier Overlapping Disposition Pulse Width Modulation*

CO-PD *Carrier Overlapping Phase Disposition*

CO-POD *Carrier Overlapping Phase Opposition Disposition*

CO-APOD *Carrier Overlapping Alternate Phase Opposition Disposition*

NLM *Nearest Level Modulation*

SHEPWM *Selective Harmonic Elimination Pulse Width Modulation*

PU *Per Unit*

FFT *Fast Fourier Transform*

IGBT *Insulated Gate Bipolar Transistor*

NR *Newton-Raphson*

PSO *Particle Swarm Optimization*

DE *Differential Evolution*

GA *Genetic Algorithms*

SA *Simulated annealing*

HS *Harmony Search*

HMCR *Harmony Memory Considering Rate*

PAR *Pitch Adjusting Rate*

HM *Harmony Memory*

THD *Total Harmonic Distortion*

ANN *Artificial Neural Networks*

INTRODUCTION

Power electronics is considered to be a revolutionary field and an essential part of electrical engineering due to the obtained insights and the discoveries made during its development. The history of power electronics began in the 1900s when mercury arc rectifiers and thyratrons were developed and used in power transmission systems. In the 1950s thyristors and silicone diodes were developed and used in different electrical systems to overcome the problems caused by the previous such as low efficiency, high manufacturing cost and high environmental risks.

A power converter is a fundamental part of almost any electric device; it allows the conversion of electrical energy form one form to another. Power converters that convert DC voltages into AC are called inverters, these converters are widely used in grid connected and AC motor driving systems[1–3].

Many commercial, industrial installations and transportation systems require high voltage to operate. Multilevel inverters were introduced in 1970s [4] these converters were developed with the aim of overcoming the problems and limitations presented by conventional converters, the topology can be simply achieved by connecting multiple semiconductor devices in series in order to lower the voltage stress. Multilevel inverters are well known for their ability to generate high voltage waveforms with low harmonic content. However, increasing the number of switching devices will result in an expensive and a complex system that is hard to maintain.

Asymmetric multilevel inverters are considered to be suitable solution to overcome the disadvantages presented by conventional multilevel inverters [5]. Asymmetric converters use different input voltage values for different parts and modules of the inverter, these

voltages are added and subtracted in such way that allows the generation of multiple voltage levels with fewer semiconductor switches.

This work investigates a new hybrid asymmetric multilevel inverter aimed for medium power and low power precision applications, the proposed topology promises a significant performance improvement and cost reduction compared to conventional asymmetric topologies.

In the first chapter we will take a look at the basic multilevel inverter topologies and also some of the recently developed topologies. We will discuss their main advantages and drawbacks. Based on this, the hybrid asymmetric multilevel power converter will be designed.

Multiple modulation methods have been developed to control multilevel power converters. In the second chapter we will take a brief look at some of the widely used modulation methods, we will focus particularly on a modulation method that is suitable for controlling high power multilevel inverters called selective harmonic elimination due to its low switching frequency and ability to produce high quality output voltage waveforms, which extends the lifetime of the electronic components.

The use of the selective harmonic elimination method requires solving a system of non-linear equations. Multiple mathematical methods have been proposed to solve these equations such as newton-raphson or resultant theory but these methods are either complicated or require guessing initial solutions which can be difficult especially for a large number of variables. Another way to solve this problem it using optimization algorithm such as genetic algorithms or particle swarm optimization, these methods are efficient and do not require initial guess of the decision variables. In the third chapter we present some of the well known and frequently used optimization methods along with a recently developed optimization method called harmony search. The chapter also investigates the application of artificial neural networks.

The neural networks are trained using data sets obtained from optimization methods, then used to control multilevel converters in real-time without the need for performing any computations. This method can be beneficial in the case of analyzing and studying

complicated systems.

In the fourth chapter we demonstrate and analyze the proposed multilevel converter, we also study the effect of combining the ability of the proposed converter of generating high number of voltage levels and the selective harmonic elimination strategy on the quality of the generated voltage waveform.

CHAPTER 1

MULTILEVEL CONVERTER TOPOLOGIES

Multilevel Direct current to alternating current (DC/AC) power conversion is a very important technology. Inverters play a critical role in machine drives, power transmission systems, induction heating, electric vehicles, and other technologies. The recent advancement in power electronic devices and the increasing demand on electrical energy have led to the development of multiple configurations of DC to AC converters. Although the several advantages and benefits that multilevel inverters provide compared to conventional two level inverters such as low electromagnetic interference and low harmonic distortion, the market penetration of these inverters is still significantly low due to high semiconductor device count. Therefore many multilevel inverter topologies with reduced device count have been developed in the last few years to address this issue. This chapter presents an overview of the fundamental converter topologies, the recently developed ones and their applications.

1.1 Fundamental topologies

1.1.1 Diode clamped multilevel converters

The diode clamped topology was first introduced in 1981 by A.Nabae et al [6]. Figure 1.1 and 1.3 shows the three and five level configurations respectively. The topology uses capacitors connected in series to generate multiple voltage levels.

A single leg is composed of four switching elements with four anti-parallel diodes. On the dc side of the converter, the dc bus capacitor is split into two, providing a neutral point N. the diodes connected to the neutral point are called clamping diodes. When the inter switching elements (for example: S_{a2} and S_{a3}) are turned on, the inverter output terminal is linked to N through one of the clamping diodes.

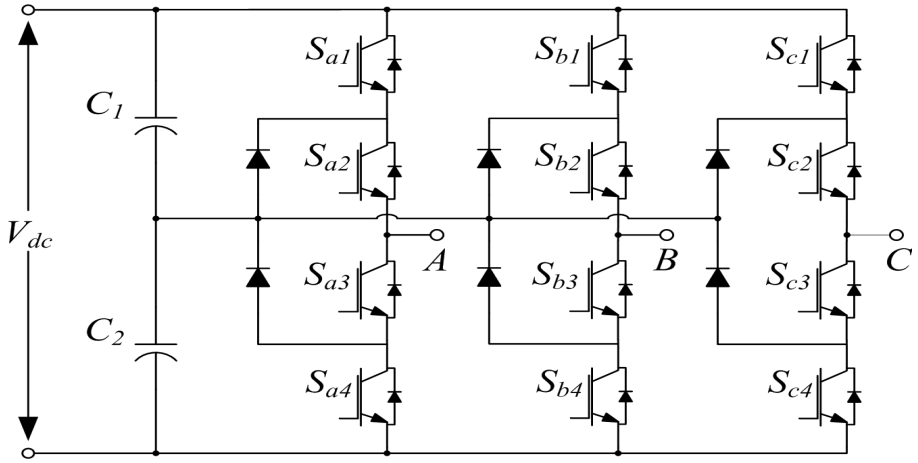

FIGURE 1.1. Three level diode clamped topology

Table 1.1 shows the possible switching states. It can be seen from the table that the switching elements S_1 and S_3 function in a complementary manner which means, if the first switch is turned on the other must be switched off. Similarly, S_2 and S_4 also operate in complementary manner.

Table 1.1: Switching States for three level diode clamped inverter.

Device Switching Status				Inverter Terminal Voltage
S_1	S_2	S_3	S_4	
On	*On*	*Off*	*Off*	V_{dc}
Off	*On*	*On*	*Off*	0
Off	*Off*	*On*	*On*	$-V_{dc}$

Figure 1.2 shows an example of a three voltage waveform generated by the inverter and gating signal arrangements. The generated waveform has three voltage levels $\frac{V_{dc}}{2}$,0 and $\frac{-V_{dc}}{2}$. V_{s1} ,V_{s2} ,V_{s3} and V_{s4} are the gating signals for S_1 to S_4 respectively.

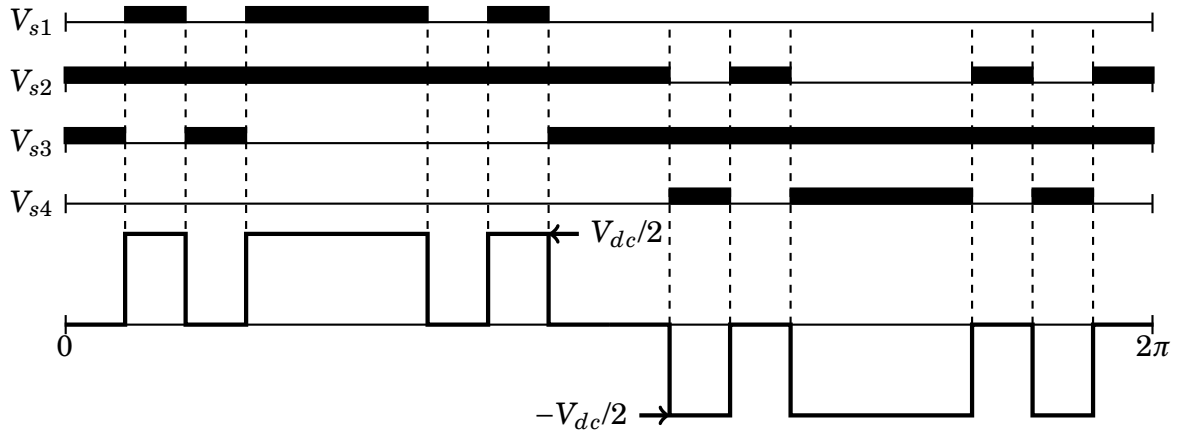

FIGURE 1.2. Gating signals, and output voltage of three level diode clamped inverter.

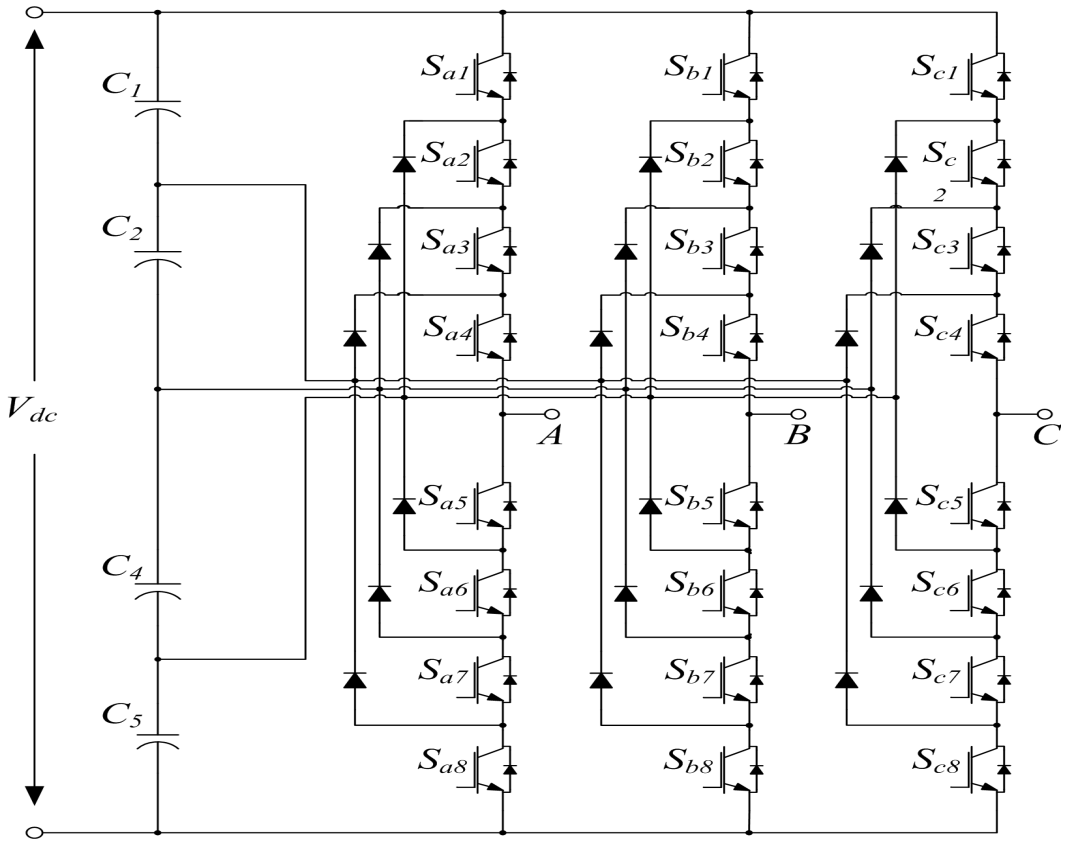

FIGURE 1.3. Five level diode clamped topology.

Although the extendibility of the diode clamped topology, the three level structure is the most used topology in the industry due to capacitor voltage balancing issues for higher number of voltage levels [7–10]. The NPC topology is mainly used for motor drive applications [11, 12], but also has been used for photovoltaic applications [13, 14] and grid applications [15, 16].

1.1.2 Flying capacitor converter

Figure 1.4 demonstrates different variants of what is called a flying capacitor multilevel converter (FCMC). The topology was first introduced in 1992 by *T.A. Meynard*, *H. Foch* in [17] .It is considered as a good alternative to the diode clamped topology. The converter is composed of multiple switching elements connected in series with capacitor or multiple capacitors connected to each leg of the converter as demonstrated in the figures. The

capacitors in this topology are not connected to the DC bus therefore it is named flying capacitor converter.

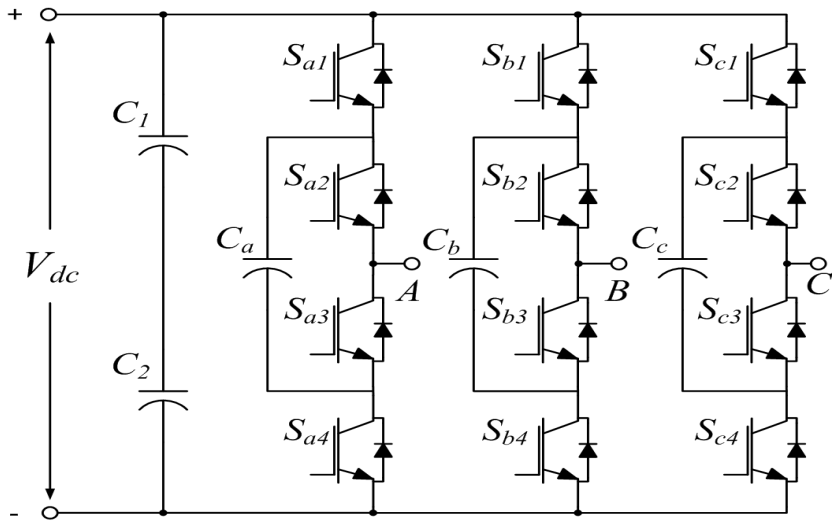

FIGURE 1.4. Three level flying capacitor topology.

The multilevel capacitor converter is a natural extension of the two level FC topology. Figure 1.5 presents the five level version of the FC topology. Each leg of this converter has six capacitor C_{x1} to C_{x6}, $x = \{a, b, c\}$ with voltage rating of $\frac{V_{dc}}{4}$, the converter can generate five voltage levels per terminal $\frac{V_{dc}}{2}, \frac{V_{dc}}{4}, 0, \frac{-V_{dc}}{4}, \frac{-V_{dc}}{2}$.

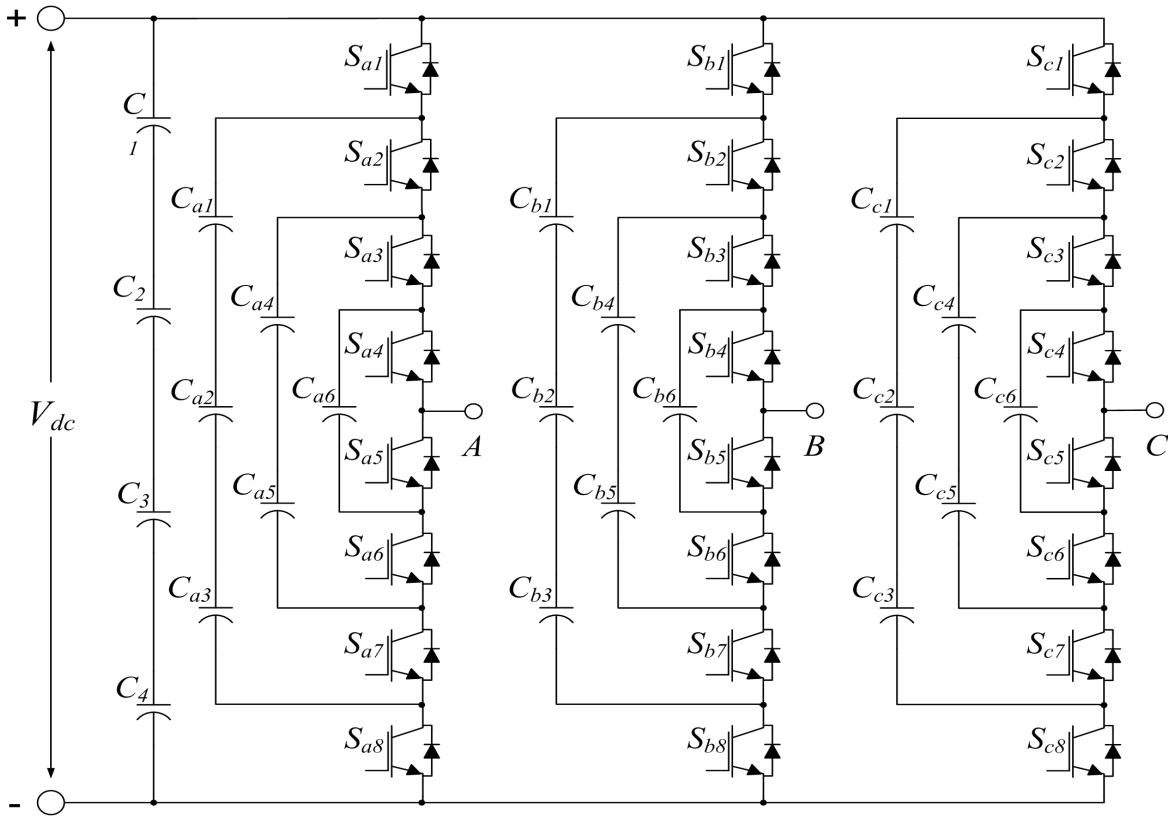

FIGURE 1.5. Five level flying capacitor topology.

Table 1.2 shows all the possible voltage levels that can be generated using the five level FC converter and the corresponding switching states.

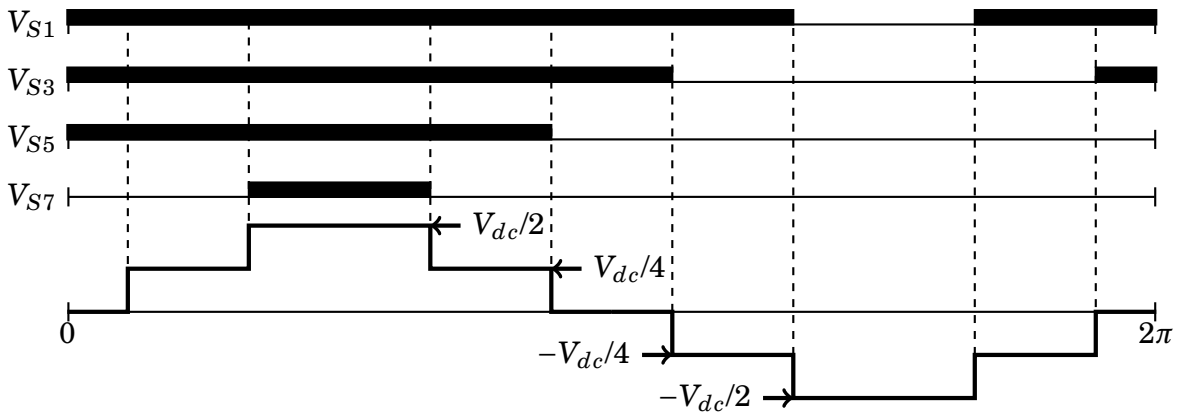

FIGURE 1.6. Five level flying capacitor wave.

It can be noticed from the table that some voltages can be generated with more than one combination.

Table 1.2: Switching States for Five level flying capacitor inverter.

Switching States				Output voltage
S1	S2	S3	S4	
On	*On*	*On*	*On*	Vdc/2
On	*On*	*On*	*Off*	Vdc/4
Off	*On*	*On*	*On*	
On	*Off*	*On*	*On*	
On	*On*	*Off*	*On*	
On	*On*	*Off*	*Off*	0
Off	*Off*	*On*	*On*	
On	*Off*	*Off*	*On*	
Off	*On*	*On*	*Off*	
On	*Off*	*On*	*Off*	
Off	*On*	*Off*	*On*	
On	*Off*	*Off*	*Off*	-Vdc/4
Off	*On*	*Off*	*Off*	
Off	*Off*	*On*	*Off*	
Off	*Off*	*Off*	*On*	
Off	*Off*	*Off*	*Off*	-Vdc/2

The main disadvantage (drawback) of this topology is the high number of capacitor required especially for larger structures and also additional circuits are required to initialize capacitors charge []. The topology has been applied in high power applications such as active power filtering [18],

1.1.3 Cascade H bridge converter

Figure 1.7 shows the Cascade H bridge (CHB) converter, the topology was first proposed in 1975 by Baker Richard H and Bannister Lawrence H [19]. As its name suggests, the converter can be formed by connecting multiple H-bridge modules in series; each module is connected to its own isolated dc power supply. Normally the DC power supplies are obtained by diode rectifiers or bidirectional DC-DC converters as figure 1.10 illustrates.

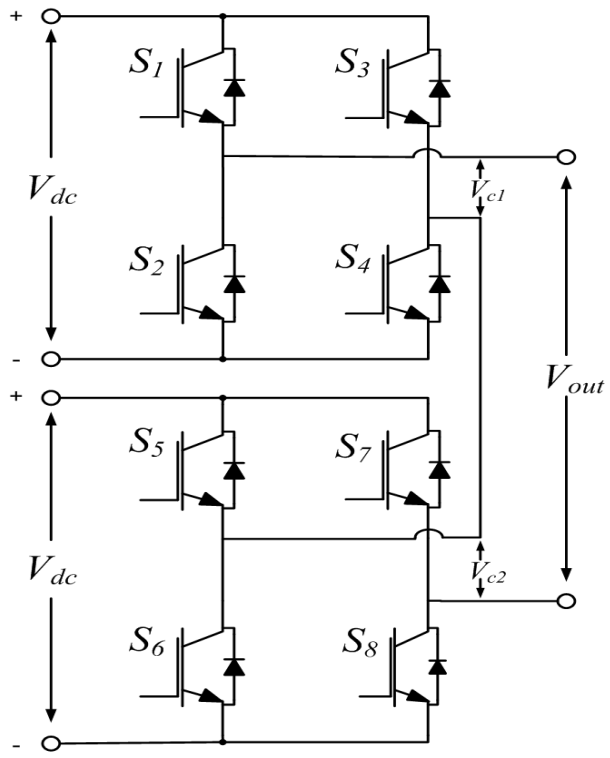

FIGURE 1.7. Single phase cascade H bridge converter topology.

The converter shown in figure 1.7 is a single phase CHB converter that generate five voltage levels. The converter is composed of two H-bridge modules connected in series the first module is formed by the switching elements S_1, S_2, S_3 and S_4 and the second one is formed by S_5, S_6, S_7 and S_8. When S_1, S_2, S_5 and S_8 are ON each of the modules generate a voltage of $V_{c1} = V_{c2} = V_{dc}$, the obtained voltage at the output is $V_{out} = V_{c1} + V_{c2} = 2V_{dc}$. On the other hand, if S_2, S_3, S_6 and S_7 are turned on the output voltage will be $-2V_{dc}$. Other levels can be generated using the switching combinations in table 1.3. The table shows only the switching states of S_1, S_3, S_5 and S_7 only,because the pairs (S_1, S_2), (S_3, S_4),(S_5, S_6) and (S_7, S_8) operate in a complementary manner in order to avoid shorting the DC power supplies. Figure 1.8 shows an example of a possible gating signals combination and the corresponding five level voltage waveform.

Table 1.3: Switching States for five level cascaded H-bridge inverter.

Device Switching Status				V_{c1}	V_{c2}	V_{aN}
S_1	S_3	S_5	S_7			
On	*Off*	*On*	*Off*	V_{dc}	V_{dc}	$2V_{dc}$
On	*Off*	*On*	*On*	V_{dc}	0	V_{dc}
On	*Off*	*Off*	*Off*	V_{dc}	0	
On	*On*	*On*	*Off*	0	V_{dc}	
Off	*Off*	*On*	*Off*	0	V_{dc}	
Off	*Off*	*Off*	*Off*	0	0	0
Off	*Off*	*On*	*On*	0	0	
On	*On*	*Off*	*Off*	0	0	
On	*On*	*On*	*On*	0	0	
On	*Off*	*Off*	*On*	V_{dc}	$-V_{dc}$	
Off	*On*	*On*	*Off*	$-V_{dc}$	V_{dc}	
Off	*On*	*On*	*On*	$-V_{dc}$	0	$-V_{dc}$
Off	*On*	*Off*	*Off*	$-V_{dc}$	0	
On	*On*	*Off*	*On*	0	$-V_{dc}$	
Off	*Off*	*Off*	*On*	0	$-V_{dc}$	
Off	*On*	*Off*	*On*	$-V_{dc}$	$-V_{dc}$	$-2V_{dc}$

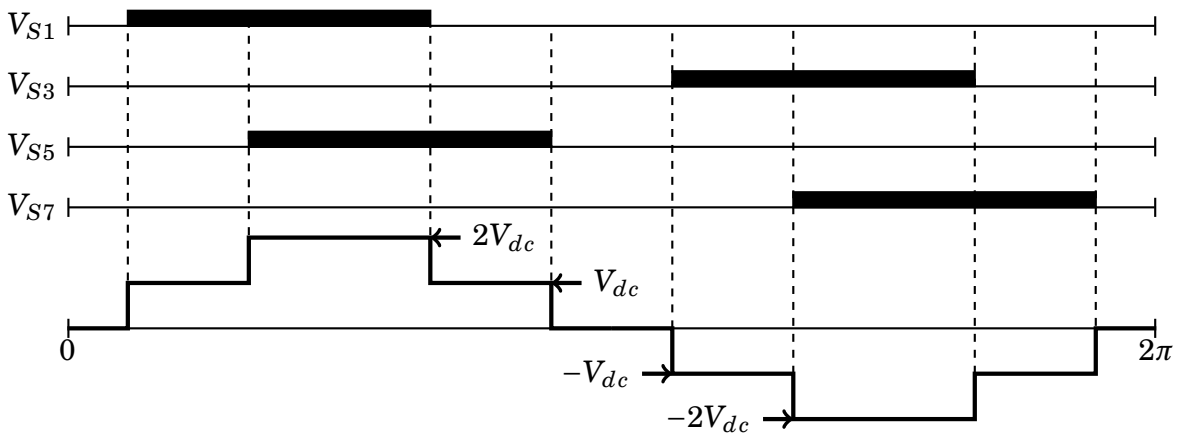

FIGURE 1.8. Gating signals, and output voltage of five level cascaded H-bridge inverter.

A three phase CHB inverter can be constructed by connecting three converters as demonstrated in figure1.9.

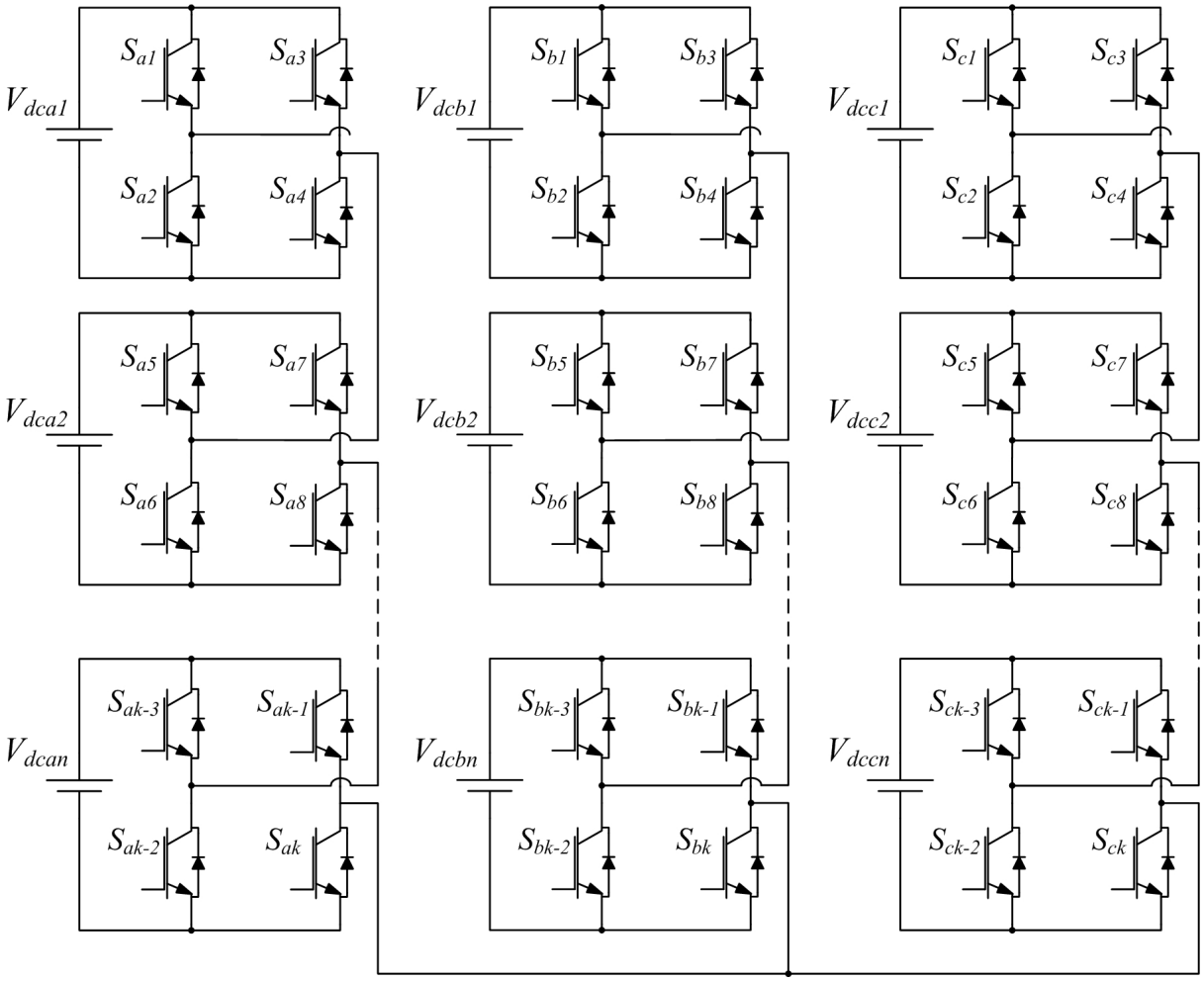

FIGURE 1.9. generalized three phase cascade H bridge converter topology.

One of the main advantages of the cascade H-bridge topology is that the control and protection mechanisms of the H-bridge modules are modular; therefore development and manufacturing costs are significantly reduced.

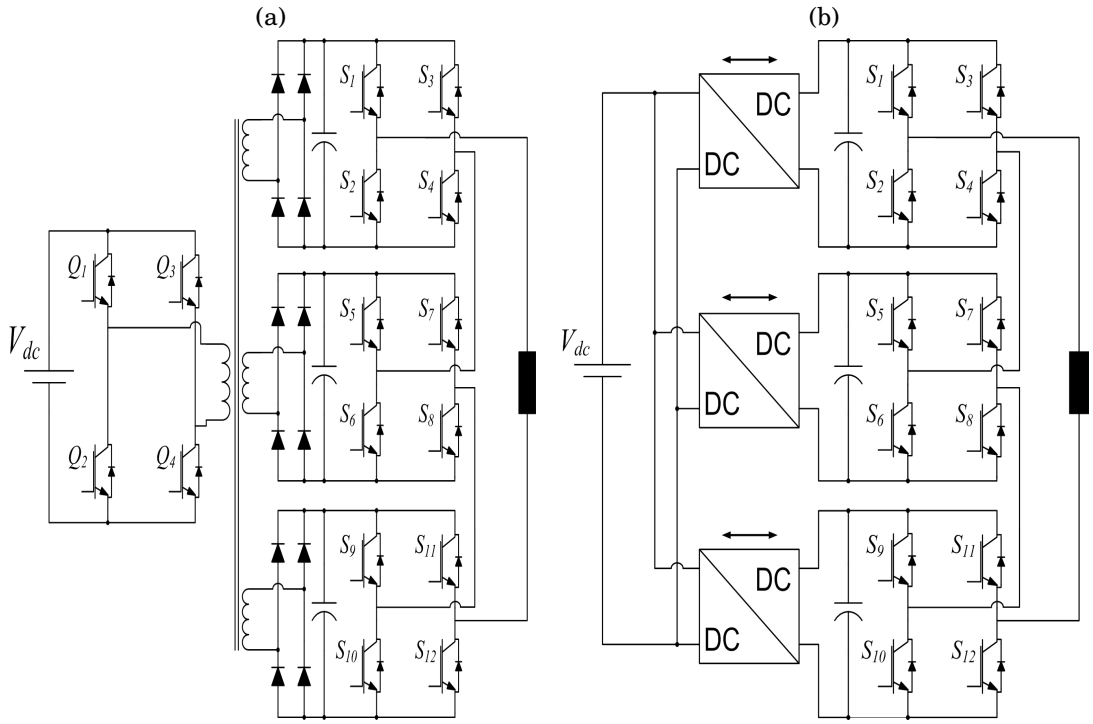

FIGURE 1.10. CHB inverter connected to different types of DC sources (a) DC sources by isolated transformers and rectifiers (b) DC sources generated by DC-DC converters.

1.1.4 Modular multi-level converter

Modular multilevel converter (MMC) topology was first proposed in 2003 by *A. Lesnicar*, it was originally designed for high voltage direct current (HVDC) transmission systems. Figure 1.11 shows a typical configuration of the modular multilevel converter topology, it is formed by connecting multiple submodules in cascade in each of the converter's arms. Figure 1.12(a) shows the basic and the widely used configuration of a submodule. The submodules can have different designs as illustrated in figure 1.12.

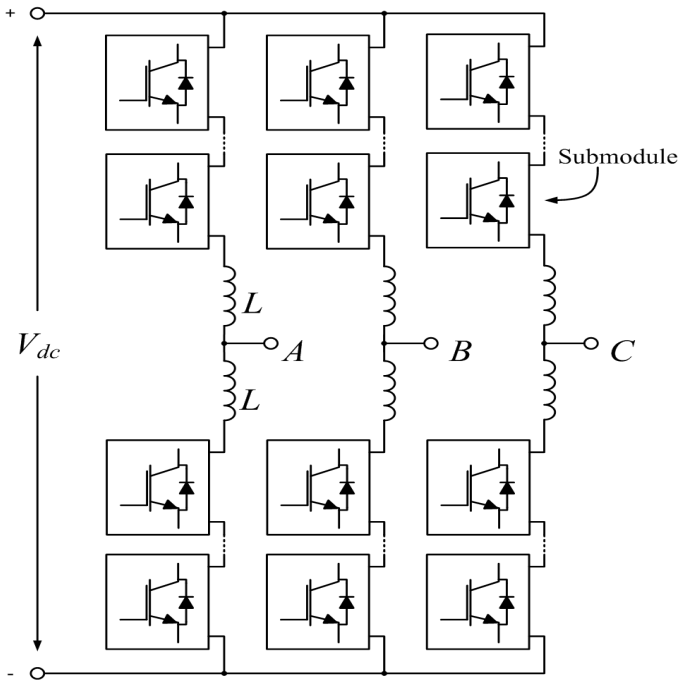

FIGURE 1.11. Genralized modular multi-level converter topology.

Unlike the CHB topology, where each H-bridge module needs an isolated power supply, the MMC submodules do not require isolated DC sources, instead the submodules use capacitors as the following figure shows. The voltage of the submodules is provided by a DC bus with a voltage of V_{dc}.

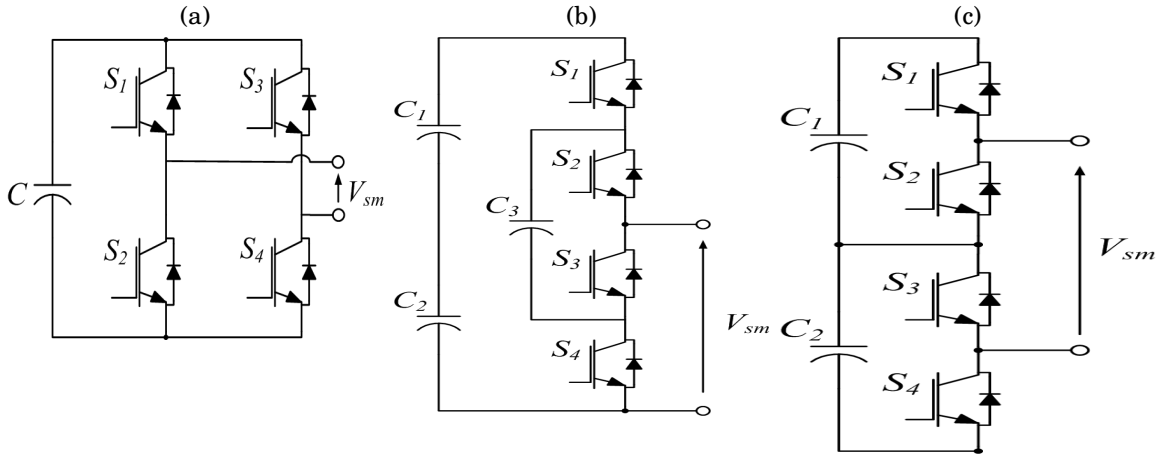

FIGURE 1.12. Other submodules configurations:(a) Full bridge, (b) flying capacitor, (c) three level submodule.

1.2 Symmetric multilevel topologies

The topologies presented previously (diode clamped, flying capacitor and cascaded H-bridge) are considered as symmetrical inverters, because the voltages across the intermediate-circuit capacitors are equal, and all the switching elements have the same voltage rating (voltage blocking capability). One of the main disadvantages of these topologies is the high number of switching devices especially for high number of voltage levels, table 1.4 compares the number of switching devices required for each topology. The switching elements are assumed to have the same power rating.

Table 1.4: Comparaison of different fundamental topologies.

	Topology	T	D	m
3 Level	diode clamped	4	6	2
	flying capacitor	4	4	2
	cascaded h bridge	4	4	2
5 Level	diode clamped	8	20	4
	flying capacitor	8	8	4
	cascaded h bridge	8	8	4
7 Level	diode clamped	12	42	6
	flying capacitor	12	12	6
	cascaded h bridge	12	12	6
m+1 Level	diode clamped	$2m$	m^2+m	m
	flying capacitor	$2m$	$2m$	m
	cascaded h bridge	$2m$	$2m$	m

It can be clearly seen form the table that the cascaded H-bridge inverter is the most advantageous topology especially for a high number of voltage levels.

1.3 Asymmetric multilevel topologies

In the recent years, the idea has risen to use multilevel asymmetric topologies with the aim of reducing the number of switching devices. Most of asymmetric multilevel inverters have almost the same structure as symmetric multilevel inverters. The only difference is the amount of input DC voltage of each module and the voltage/current rating of the

switching components. However the proprieties of these topologies are different such as the number of voltage levels generated.

Asymmetric converters have the ability to generate the same number of voltage levels as the symmetric topologies but with less switching elements, which increases their reliability.

Figure 1.13 shows the symmetric (right) and asymmetric (left) nine level configurations. It can clearly observed from the figure that the asymmetric topology uses way less switching elements than the symmetric version. It can be also noticed that the H-bridge modules in the asymmetric topology use different DC voltages. With unequal input dc sources, the number of generated levels can be increased without necessarily adding more modules. This combination is actually one possible case out of several. Other combinations can be made using this configuration.

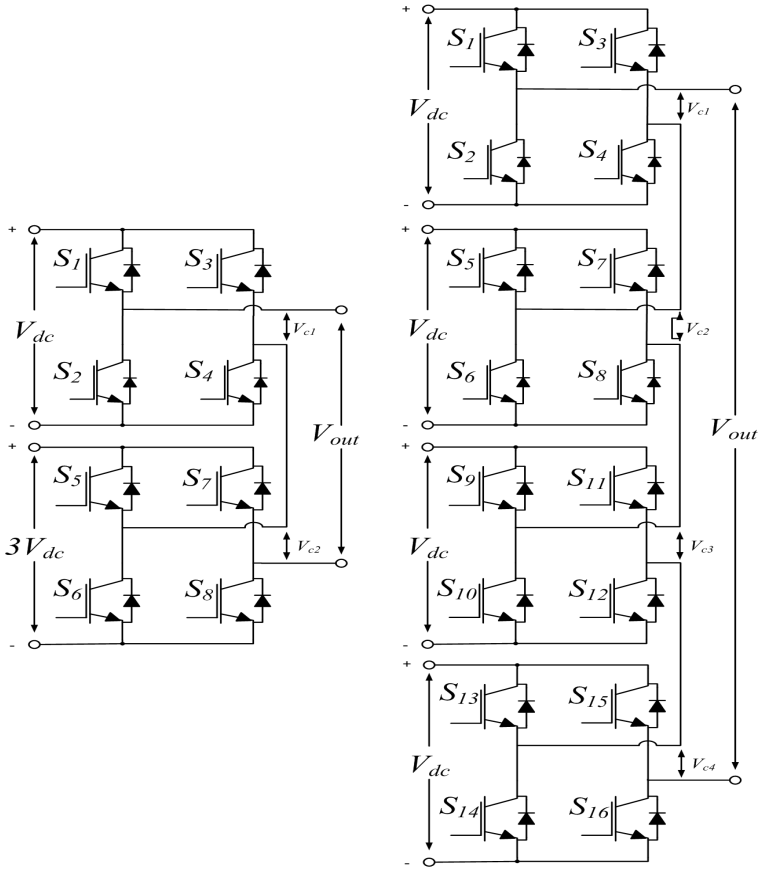

FIGURE 1.13. Single phase cascade H .

The process of designing an asymmetrical converter can be generalized. The first step towards designing a converter is modeling the basic structure that makes it which is the H-bridge module. An H-bridge module can be controlled only using four switching combinations,two of these combinations generate the same output voltage level as demonstrated in figure 1.14.

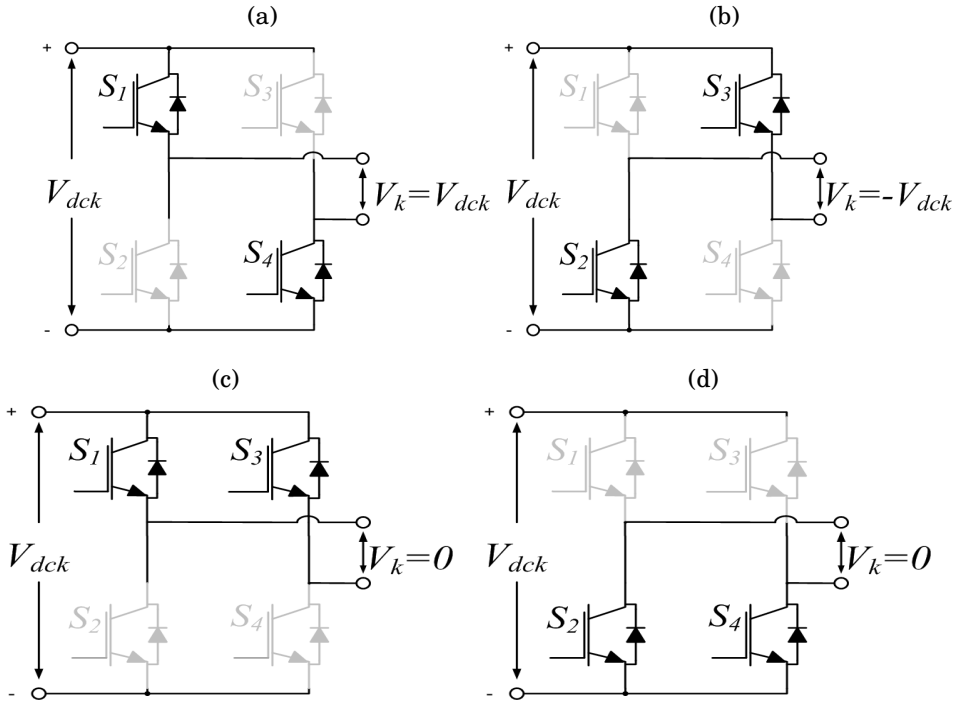

FIGURE 1.14. Possible voltages generated by a single H-bridge module.

The voltages that can be generated from the module are three, the positive voltage, the negative voltage and zero volt. The voltage generated by k module can be expressed by the following equation :

$$V_k = S_k \times V_{dck} \quad with\ S_k \in \{-1, 0, 1\} \tag{1.1}$$

where S_k is the switching state and V_{dck} is the input voltage of the H bridge module. The overall voltage generated by k modules relative to reference point can be computed by summing the voltages generated by each module as the following expression indicates:

$$V_o = \sum_{i=1}^{k} V_{ci} \tag{1.2}$$

The following equation allows us to compute the number of voltage levels N, which depends on the number of modules and the the corresponding voltage sources.

$$N = 2 \times \left(\sum_{i=1}^{k} V_{dci} \right) + 1 \tag{1.3}$$

A tree of output voltages can be constructed in order map every possible module combination. The nine level configurations shown previously in figure 1.13 are taken as an example. The tree starts with the reference point (the 0V point). Three branches are then extended from the reference point to the next possible voltages generated by the first module. Other branches are then drawn from the voltages generated from the first to the ones generated by the next cell. This process goes on in a similar manner until the maximum number of possible voltages is reached.

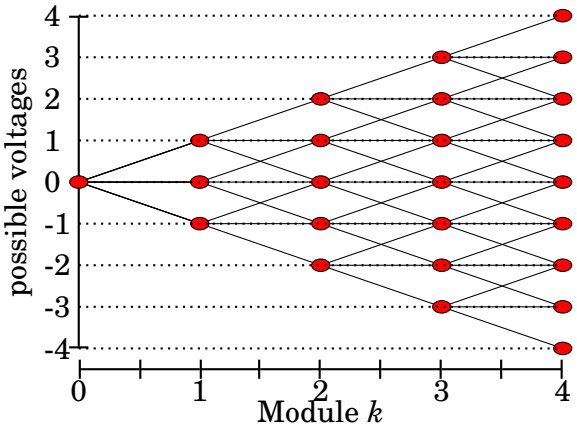

FIGURE 1.15. Possible output voltages per unit (P.U.) using nine level H-bridge symmetric topology .

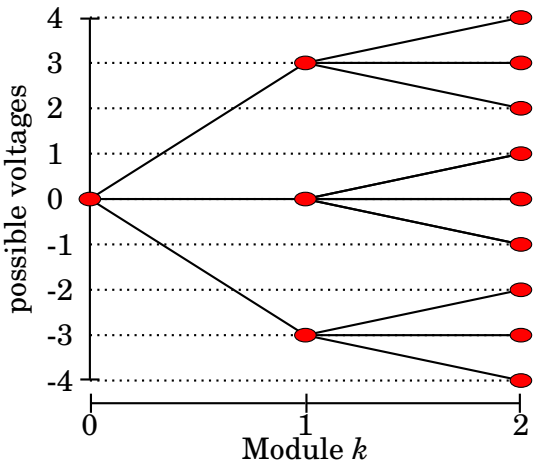

FIGURE 1.16. Possible output voltages per unit (P.U.) using nine level H-bridge asymmetric topology.

Figure 1.15 and figure 1.16 illustrate the possible voltages can be generated using symmetric and asymmetric nine level converters.. It can be noticed from the figures that [some] branches in the symmetric configuration lead to the same voltage levels, which means that the symmetric configuration has many redundant states.

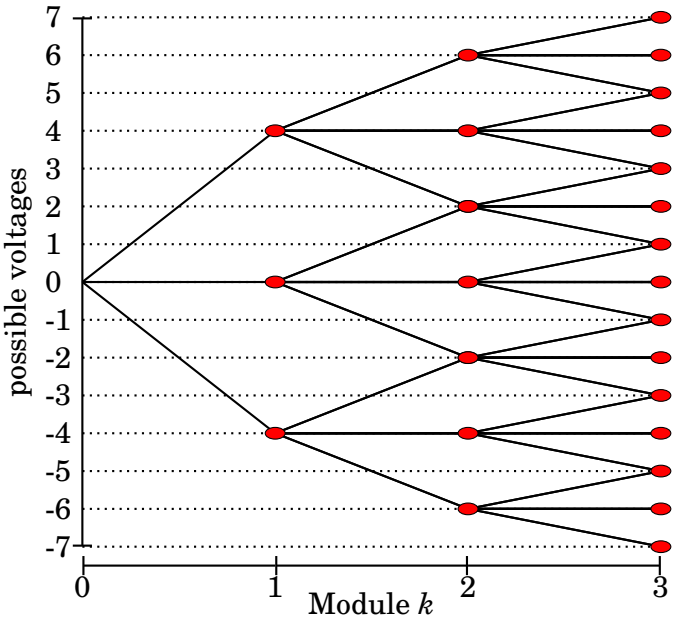

FIGURE 1.17. Possible output voltages of each H-bridge module to generate 15 levels using k=3

Obviously the topology can be extended beyond two modules, table 1.5 shows some examples of possible voltage combinations using three H-bridge modules, it can be seen from the table that the minimum number of voltage level can be produced 15, whereas the maximum number of voltages is 21.

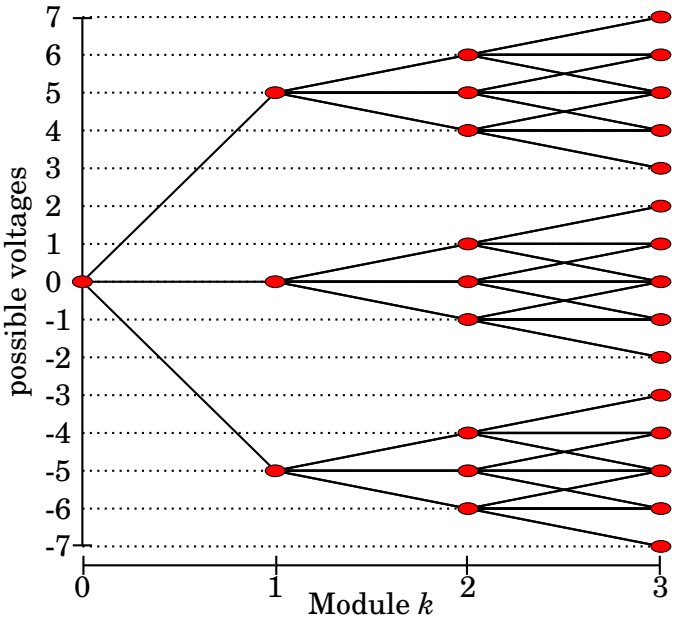

FIGURE 1.18. Possible output voltages of each H-bridge module to generate 15 levels using k=3

Figures 1.17, 1.18 and 1.19 show the possible voltages that can be generated using k=3 H bridge modules with DC voltages ($V_{dc1} = 1, V_{dc2} = 2, V_{dc3} = 4$), ($V_{dc1} = 1, V_{dc2} = 1, V_{dc3} = 5$) and ($V_{dc1} = 1, V_{dc2} = 2, V_{dc3} = 7$) respectively.

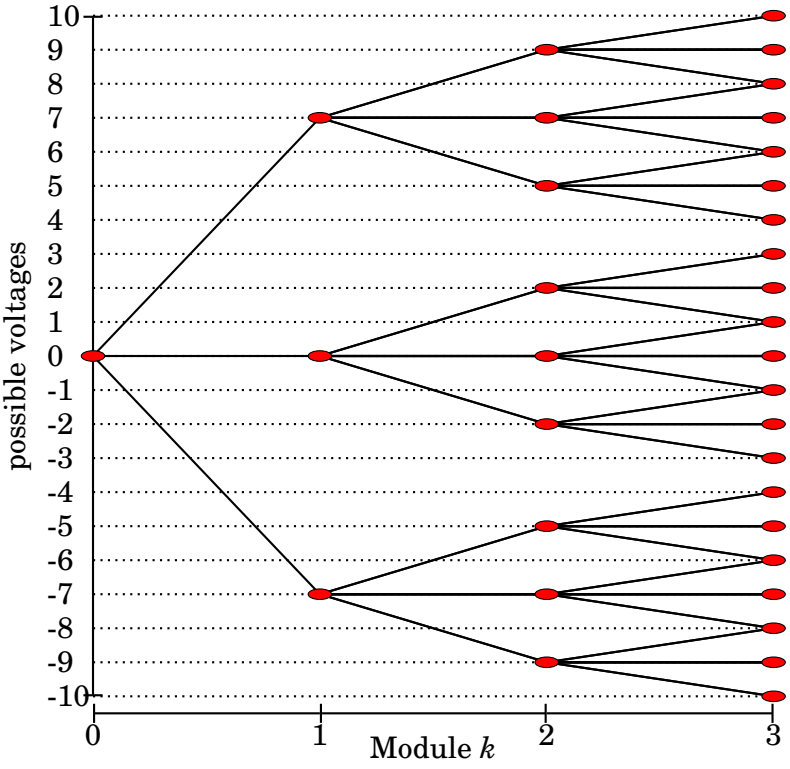

FIGURE 1.19. Possible output voltages of each H-bridge module to generate 21 levels using k=3

Table 1.5: Examples of unequal DC-voltages.

V_{dc1}	V_{dc2}	V_{dc3}	m
1	1	5	15
1	3	3	15
1	2	4	15
1	2	7	21
1	3	6	21

1.4 Hybrid Topologies:

In spite of their success, classical topologies (diode clamped, flying capacitor and CHB converter) have multiple drawbacks such as high switching device count and circuit complexity. Hybrid multilevel topologies have been proposed to overcome these problems. Hybrid converters combine the advantages provided by the different basic topologies.

1.4.1 DC-AC cascaded H-bridge multilevel boost converter

The DC-AC cascaded H-bridge multilevel boost converter was first introduced in 2009 by zhong du et al [20] , the topology of the proposed converter is shown in figure 1.20, the converter consists of a simple two level three legged inverter, each leg is connected to an H-bridge module, the DC supply to the modules is provided by capacitors

The topology was proposed to overcome the problem of inefficiency caused by inductors in boost DC-DC converters destined for electric vehicles. It must be noted that for some applications the capacitors connected to the H-bridge modules can be replaced with DC sources [21].

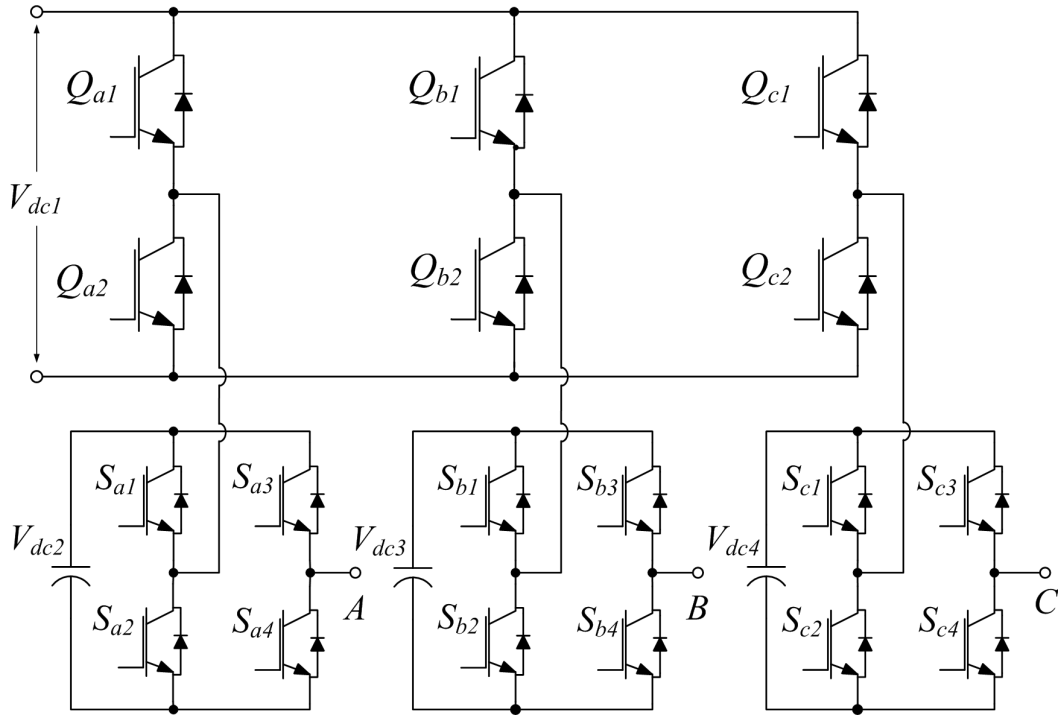

FIGURE 1.20. Single phase cascade H bridge converter topology.

1.4.2 Cascaded npc

The hybrid multilevel inverter shown in figure 1.21 is a combination of neutral point clamped inverter and cascaded H-bridge topology, the main advantage of this topology is the reduction of required isolated DC sources compared to a conventional cascaded

H-bridge inverter [22]. Each module can generate five voltage level, therefore the overall number of voltages generated is nine.

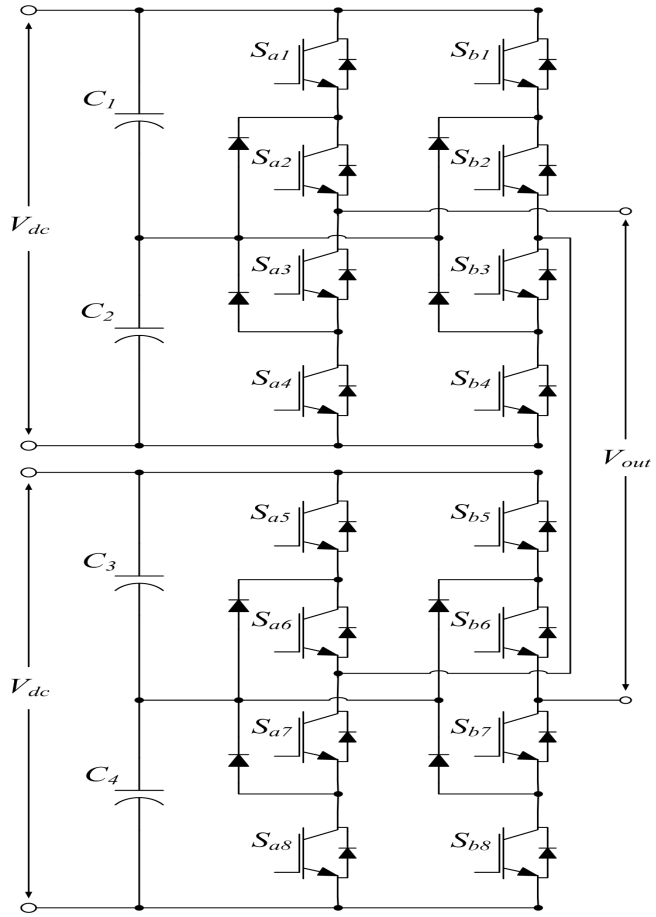

FIGURE 1.21. hybrid multilevel inverter.

1.4.3 Nested Neutral Point-Clamped topology

Nested Neutral Point Clamped multilevel Converter (NNPC) is a combination of the neutral point clamped topology (NPC) and the flying capacitor topology (FC). . Figure 1.22 shows the three phase four level NNPC topology. Each leg consists of six switching elements S_1 to S_6 connected series, two capacitors and two diodes. The FC topology is formed by the inner components: S_1 S_2, S_5,S_6 and the two capacitors, whereas the NPC topology is formed by the inner components: S_2,S_3, S_4,S_5 and the two diodes. The switching elements S_2 and S_5 are shared by both topologies.

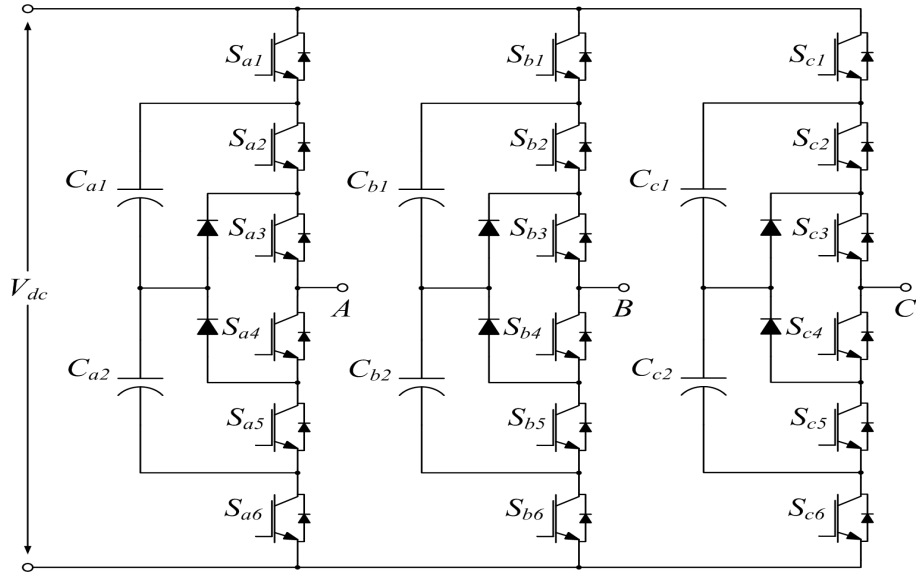

FIGURE 1.22. Nested Neutral Point-Clamped topology

In order to generate the desired four voltage levels, the capacitors C_{x1} and C_{x2} with $x = a, b, c$, must be kept at $\frac{V_{dc}}{3}$. Table 1.6 shows the switching states for the four level NNPC inverter, it can be observed from the table that the pairs (S_1, S_6), (S_2, S_4), and (S_3) S_5) work in a complementary manner. With these switching states the inverter can generate four voltage levels $\frac{V_{dc}}{2}$, $\frac{V_{dc}}{6}$, $\frac{-V_{dc}}{6}$ and $\frac{-V_{dc}}{2}$.

Table 1.6: Switching states for 4L NNPC.

Switching States						Output voltage
S_1	S_2	S_3	S_4	S_5	S_6	
On	*On*	*On*	*Off*	*Off*	*Off*	$V_{dc}/2$
On	*Off*	*On*	*On*	*Off*	*Off*	$V_{dc}/6$
Off	*On*	*On*	*Off*	*Off*	*On*	
On	*Off*	*Off*	*On*	*On*	*Off*	$-V_{dc}/6$
Off	*Off*	*On*	*On*	*Off*	*On*	
Off	*Off*	*Off*	*On*	*On*	*On*	$-V_{dc}/2$

1.5 Topologies with reduced device count:

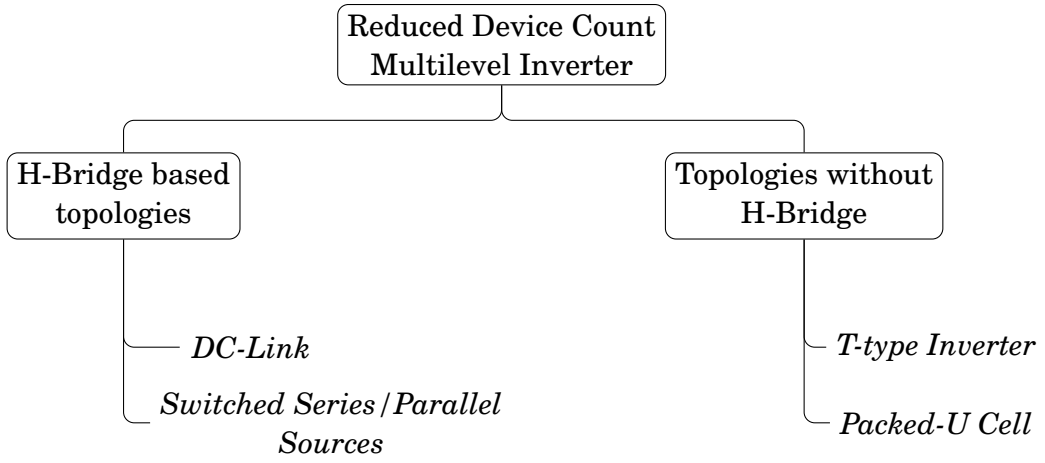

FIGURE 1.23. Categorization of Multilevel inverter topologies with reduced device count

1.5.1 Topologies without H-bridge

Reduced device count multilevel inverter without H-bridge topologies have the ability to generate an AC voltage waveform directly from multiple DC sources and switching elements. The T-type and Packed U-cell converter are two of the most widely known topologies in this category.

1.5.1.1 T-type multilevel inverters

The topology shown in figure 1.24 which presents a five level inverter was first proposed in 2006 by *G. Ceglia* et al [23]. the topology presents a significant reduction in the number of switching elements comparing to a conventional five level inverter. The topology consists of two main parts an H-bridge converter formed by S_1,S_2,S_3 and S_4, and a bidirectional switch.

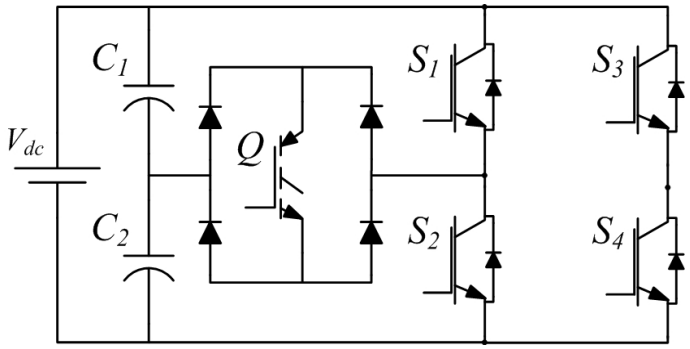

FIGURE 1.24. Five level inverter with reduced device count.

Table 1.7: Output voltage levels with corresponding conducting switches for the five level inverter proposed by Cegia.

V_{out}	**Switches in (ON) state**
0	S_1,S_2,S_3,S_4
1	S_1,S_2,S_3,S_4
2	S_1,S_2,S_3,S_4
3	S_1,S_2,S_3,S_4
4	S_1,S_2,S_3,S_4
5	S_1,S_2,S_3,S_4

A capacitor voltage divider formed by C_1 and C_2 allows the generation of two voltage levels from a single DC voltage source. Table shows all the switching states of the topology. The topology can be extended to beyond 5 levels []; figure demonstrates a generalized topology of the converter.

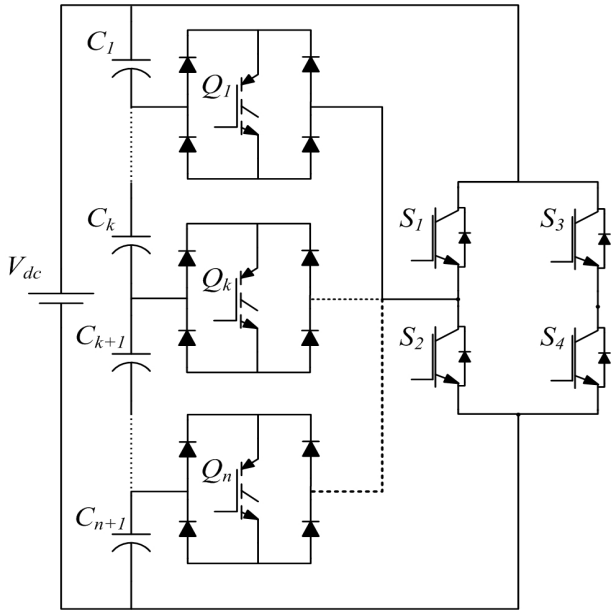

FIGURE 1.25. generalized Cegia topology.

1.5.1.2 Packed U-cell multilevel inverter

Packed U-cell multilevel inverter topology was first introduced in 2011 by *Al-Haddad et al.* Figure 1.26 shows a seven level version of the converter, it consists of six switching elements S_1 to S_6, an isolated voltage source and a capacitor. Table 1.8 shows the switching table for the topology. The pairs of switching elements (S_1,S_4), (S_2,S_5) and (S_3,S_6) work in complementary manner.

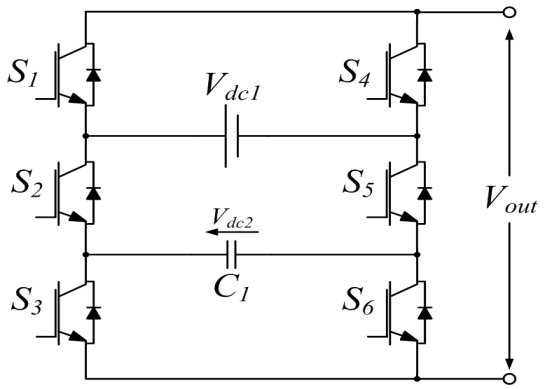

FIGURE 1.26. Single-phase PUC inverter.

Table 1.8: Switching states for 7L PUC.

Switching states			V_{out}
S_1	S_2	S_3	
On	*Off*	*Off*	V_{dc1}
On	*Off*	*On*	$V_{dc1} - V_{dc2}$
On	*On*	*Off*	V_{dc2}
On	*On*	*On*	0
Off	*Off*	*On*	$-V_{dc2}$
Off	*On*	*Off*	$V_{dc2} - V_{dc1}$
Off	*On*	*On*	$-V_{dc1}$

1.5.2 H-bridge based topologies

An H-bridge based topology is usually based of two parts; the first part is a series of voltage sources and semiconductor switching elements connected in various configurations, their role is to synthesize a staircase shaped waveform. The second part of the topology is the H-bridge converter, its role is to change the polarity of the voltage waveform created previously in such a way that allows us to obtain an AC voltage waveform.

1.5.2.1 Multilevel DC link inverter (MLDCLI)

In 2005 Gui-Jia Su [24] introduced a converter topology with reduced switching device count figure 1.27(a) presents a generalized version of the proposed topology, which consists of an H-bridge (formed by S_1 to S_4) connected to multilevel DC source, the main role of the bridge is to control the polarity of the source and to create the zero voltage (0V). The multilevel DC source is formed by connecting multiple half bridge cells each cell is controlled by two switching elements. The two switching elements T and Q are operated in complementary mode, the Q switching elements are used to bypass the voltage sources whereas T switches are used to add voltage levels.

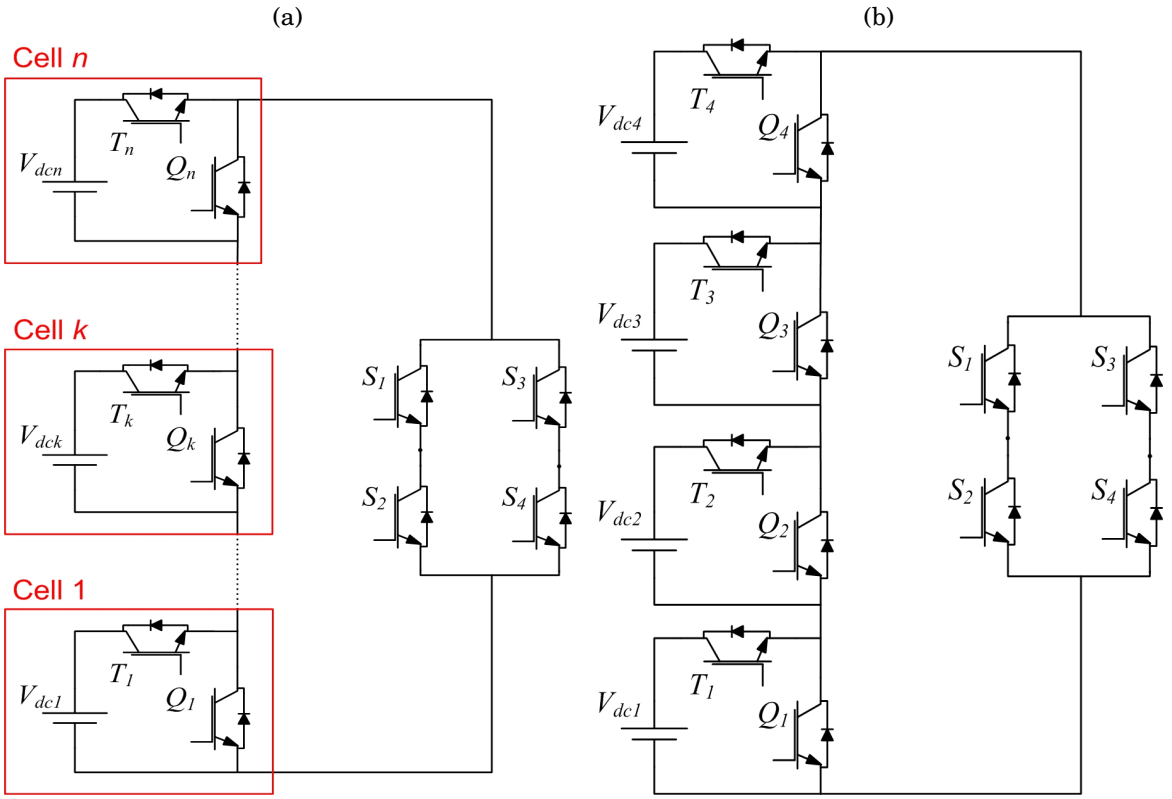

Table 1.9: Output voltage levels with corresponding conducting switches for the thirty-one level MLDCL inverter.

V_{DCbus}	**Switches in (ON) state**	V_{DCbus}	**Switches in (ON) state**
0	Q_1,Q_2,Q_3,Q_4	$V_{dc2}+V_{dc3}$	Q_1,T_2,T_3,Q_4
V_{dc1}	T_1,Q_2,Q_3,Q_4	$V_{dc2}+V_{dc4}$	Q_1,T_2,Q_3,T_4
V_{dc2}	Q_1,T_2,Q_3,Q_4	$V_{dc3}+V_{dc4}$	Q_1,Q_2,T_3,T_4
V_{dc3}	Q_1,Q_2,T_3,Q_4	$V_{dc1}+V_{dc2}+V_{dc3}$	T_1,T_2,T_3,Q_4
V_{dc4}	Q_1,Q_2,Q_3,T_4	$V_{dc2}+V_{dc3}+V_{dc4}$	Q_1,T_2,T_3,T_4
$V_{dc1}+V_{dc2}$	T_1,T_2,Q_3,Q_4	$V_{dc1}+V_{dc3}+V_{dc4}$	T_1,Q_2,T_3,T_4
$V_{dc1}+V_{dc3}$	T_1,Q_2,T_3,Q_4	$V_{dc1}+V_{dc2}+V_{dc4}$	T_1,T_2,Q_3,T_4
$V_{dc1}+V_{dc4}$	T_1,Q_2,Q_3,T_4	$V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}$	T_1,T_2,T_3,T_4

The MLDCLI topology presents a significant reduction in the number of switching elements compared to conventional cascaded H-bridge inverter. Figure 1.27(b) presents a thirty-one level MLDCL inverter with four cells, the valid switching states are shown in Table 1.9.

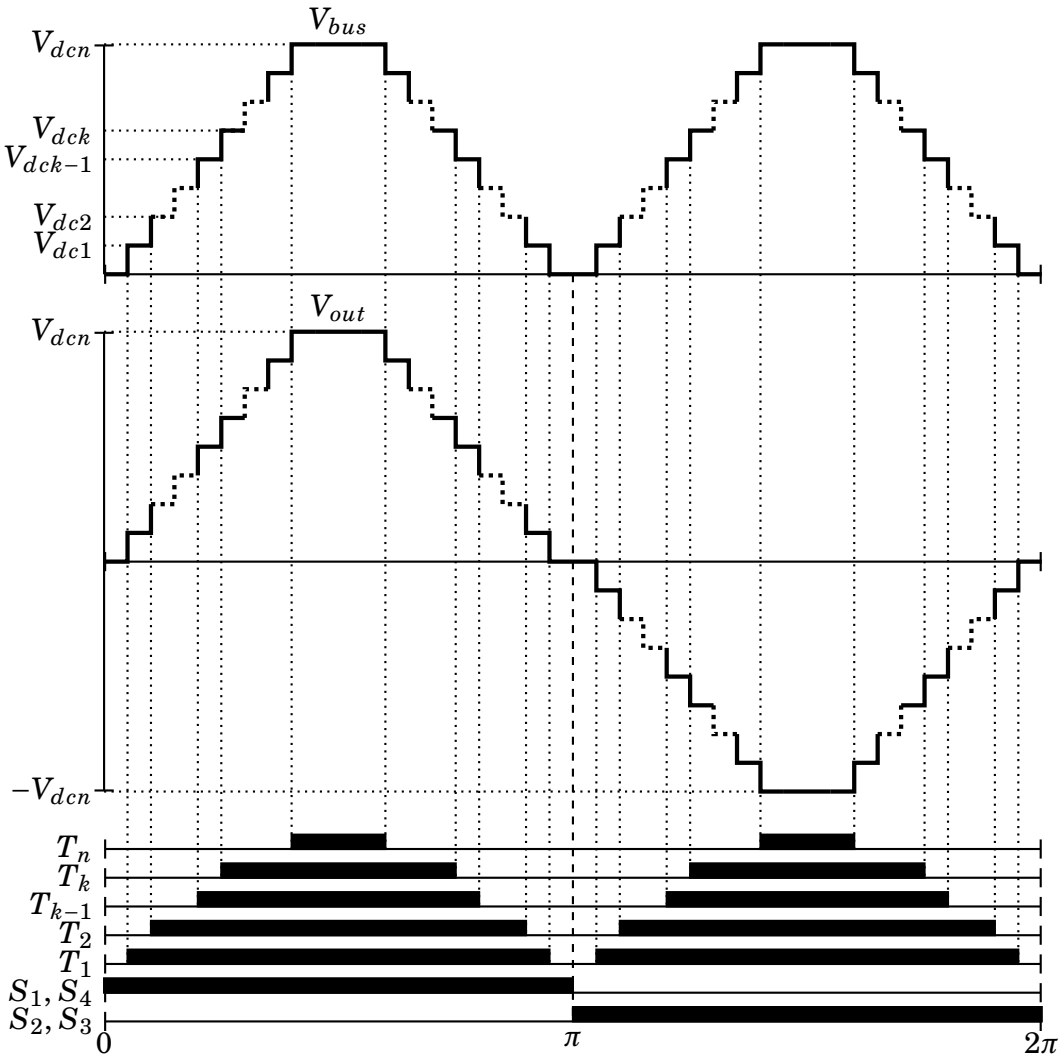

FIGURE 1.27. DC bus and output voltage waveform generated by the DC link CHB inverter

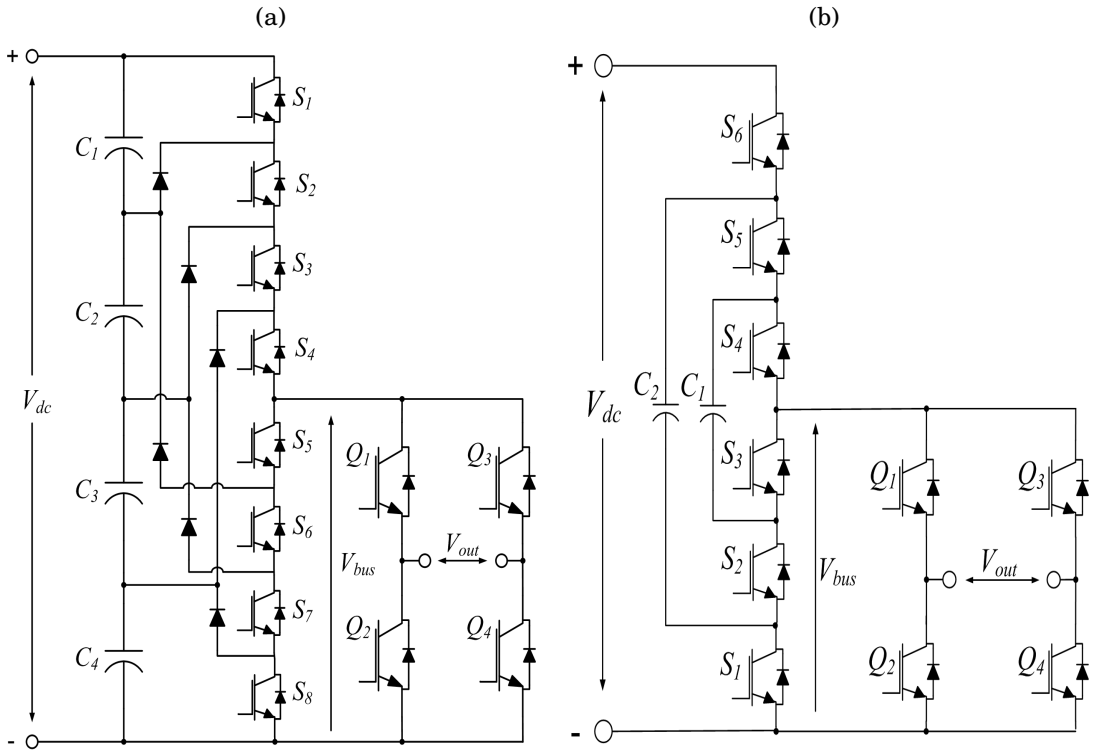

FIGURE 1.28. Generalized form of the multilevel DC link inverter (a) and the 31 level DC link inverter (b)***.

1.5.2.2 Switched series/parallel sources (SSPS) multilevel topology

The Switched series/parallel sources multilevel inverter topology was introduced in 2009 by Hingo and Kiozumi [25–27]. Figure 1.5.2.2 presents the proposed SSPS topology. The converter is composed of two parts, the voltage generation and the polarity-generation. The voltage generation part is formed by voltage sources such as batteries or capacitors and switching elements Q_1 to Q_9, the different voltage levels are generated by turning on the switching elements in series or in parallel. The polarity part is an H-bridge formed by S_1,S_2,S_3 and S_4. The valid switching states are shown in Table 1.10

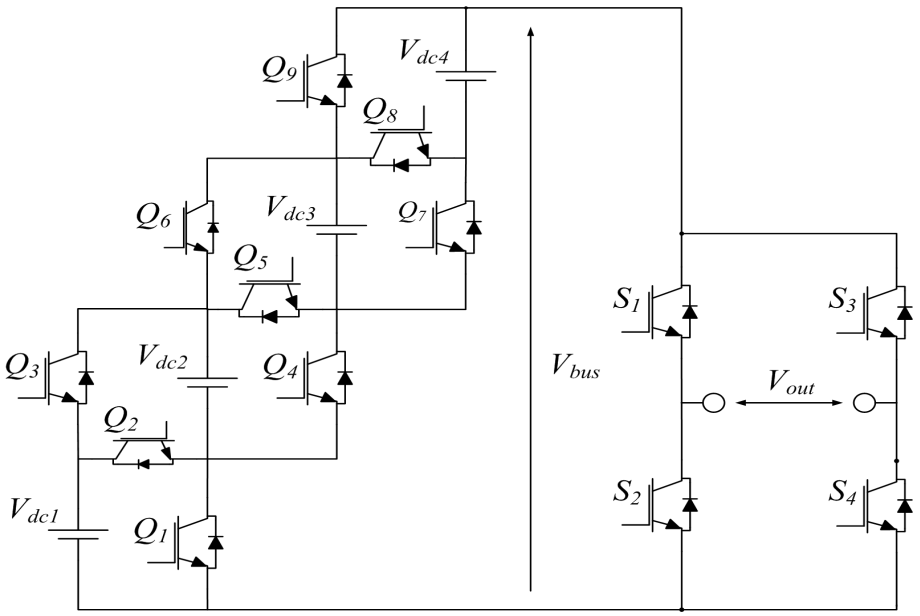

FIGURE 1.29. Switched series/parallel topology

Table 1.10: Output voltage levels ($p.u.$) with corresponding conducting switches for the proposed 21-level inverter.

Voltage ($p.u.$)	**Switches in (ON) state**	**Voltage ($p.u.$)**	**Switches in (ON) state**
10	S_1,S_4,S_{p1},S_{p4}	-1	S_3,S_5,S_{p2},S_{p4}
9	S_4,S_5,S_{p1},S_{p4}	-2	S_3,S_6,S_{p2},S_{p4}
8	S_4,S_6,S_{p1},S_{p4}	-3	S_2,S_3,S_{p2},S_{p4}
7	S_2,S_4,S_{p1},S_{p4}	-4	S_1,S_4,S_{p2},S_{p4}
6	S_3,S_5,S_{p1},S_{p4}	-5	S_4,S_5,S_{p2},S_{p4}
5	S_3,S_6,S_{p1},S_{p4}	-6	S_4,S_6,S_{p2},S_{p4}
4	S_2,S_3,S_{p1},S_{p4}	-7	S_2,S_4,S_{p2},S_{p4}
3	S_1,S_4,S_{p2},S_{p4}	-8	S_3,S_5,S_{p2},S_{p4}
2	S_4,S_5,S_{p2},S_{p4}	-9	S_3,S_6,S_{p2},S_{p4}
1	S_4,S_6,S_{p2},S_{p4}	-10	S_2,S_3,S_{p2},S_{p4}
0	S_2,S_4,S_{p2},S_{p4}		

1.6 Applications of multilevel inverters

Multiple multilevel inverter topologies are commercially available for High and medium power and applications. They come in a wide variety of standard and customized products. The neutral point clamped and NPC based hybrid topologies have found an important

market in high power adjustable speed drive applications like conveyors, pumps, fans and many other applications which offer solutions for various industries such as oil and gas, mining and marine industry. On the other hand, inverters based on flying capacitor topology have been successfully commercialized as medium voltage traction drives. Converters based on the cascaded topology have found an important market in very high power applications due to their modular nature and their capability of handling very high voltages. These topologies have been also proposed for active filtering applications and electric vehicles. This section presents some of these applications.

1.6.1 Electric vehicles

In the recent few years, hybrid and electric vehicles have been considered to be viable replacements to conventional vehicles due to their high efficiency and low carbon emissions. A hybrid electric vehicle driving system combines the use of internal combustion engines ($ICEs$) with electric motors and batteries. This combination offers the benefits provided by the electric motors such as efficiency and low carbon emissions, and the conventional ICEs such as the extended range and the ability to refuel in few minutes. From a structural point of view a hybrid electric vehicle (HEV) with a suitable internal combustion engine and sufficiently sized battery pack allows the use of either series topology or parallel topology. Heavy duty hybrid electric vehicles such as tractor or military combat vehicles usually large electric motors that require a large number of batteries and advanced electronic power converters in order to deliver the high electrical power required for them. As mentioned in the previous sections, multilevel inverters structures allow us to synthesize high quality and high voltage waveforms, for this reason multilevel inverters are suitable for high power drive systems.

Figure 1.30 shows the parallel topology of HEV motor driving system, it consists of an internal combustion engine (ICE), electric motor (motor / generator) and multiple batteries. In this configuration the wheels can be driven either by the ICE or the electric motor. Multilevel cascaded inverter topology is used in this configuration to drive the electrical motor. In driving mode the electrical power flows from the batteries to the mo-

tor,and in charging mode (from grid) the multilevel converter act as a rectifier electrical power flows grid to the batteries. The electric motor and the multilevel converter can be used to collect generated electrical power in case of breaking, in this case electric motor will act as a generator and multilevel converter will act as a rectifier to charge the batteries.

Figure 1.31 shows what is known as a series configuration, as the name suggests the two energy sources which are : the internal combustion engine and battery pack (or capacitors as demonstrated) are combined in succession. It can be seen from the figure that the electric motor MG is connected directly to the differential which makes it the only traction source, making it an electric-intensive vehicle, more suitable in urban environment. the internal combustion engine is used to drive the electric generator to maintain battery charge, by meeting the predetermined state of charge (SOC) requirements. As it can be seen from the figure, the series configuration uses two level npc converters in what is known as back to back configuration the converter on the generator's side is used as a controlled rectifier to control the amount of energy flowing from the generator the batteries. the converteron the motor side can not only be used to control the motor MG but also can be used to recover the energy generated from the motor/generator in case of breaking, the converter in this situation will act as rectifier to charge the batteries.

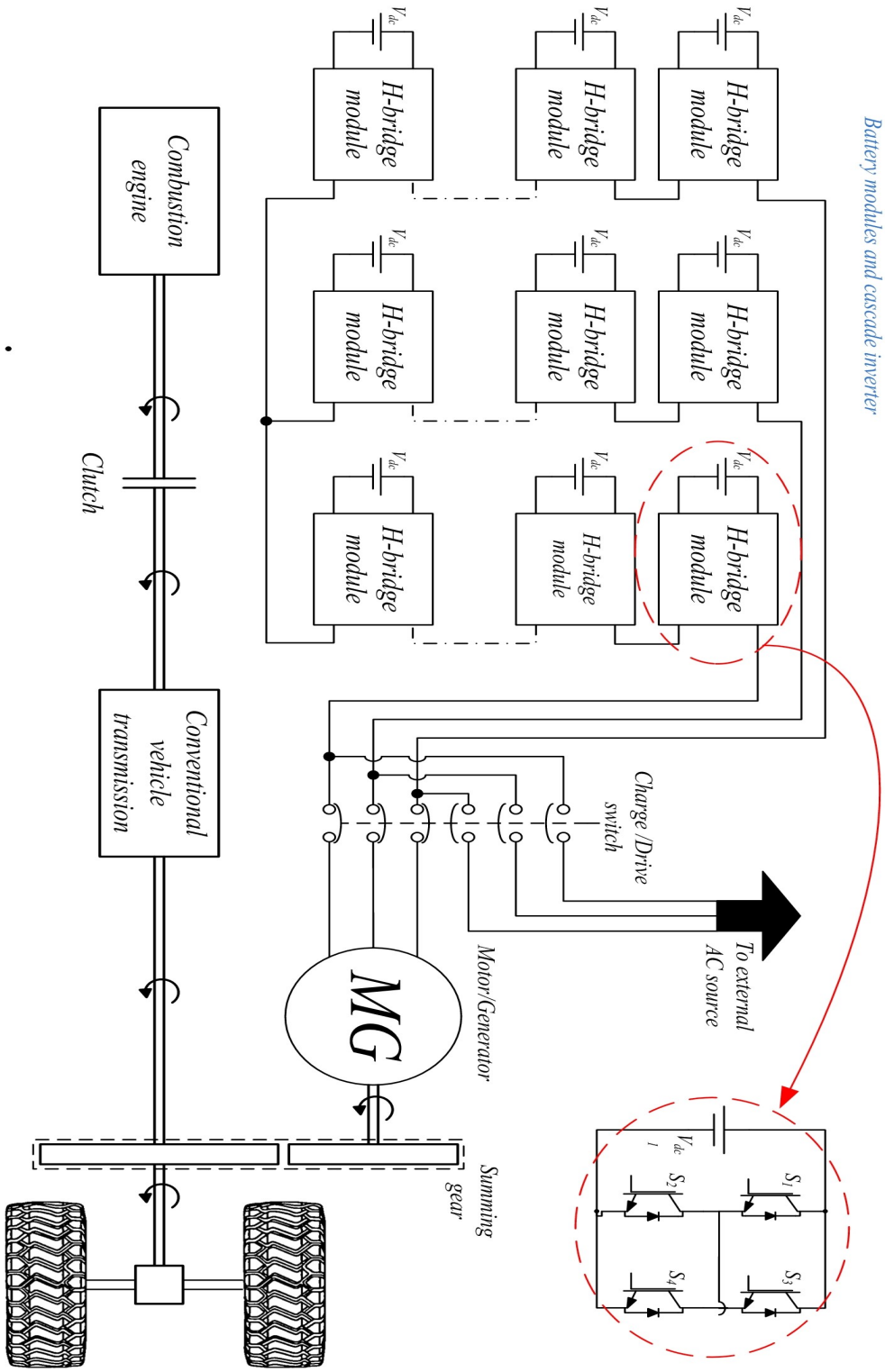

FIGURE 1.30. H-bridge drive system for EV

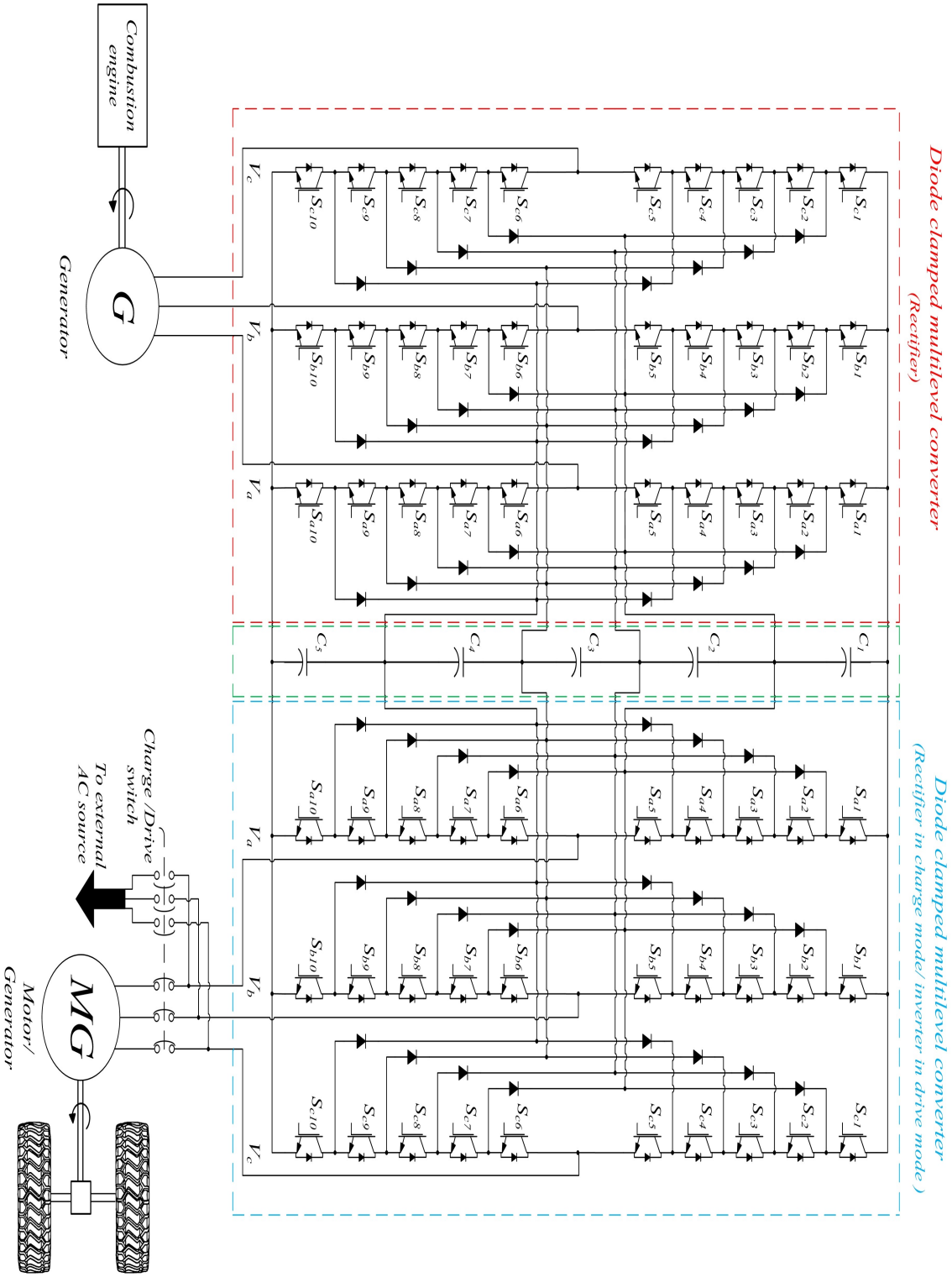

FIGURE 1.31. NPC drive system for EV

1.6.2 Photo-voltaic systems

In the recent years, the interest in using solar panels to generate electricity has significantly and rapidly increased due to environmental concerns and the rapid development in semiconductor technology which lowered the manufacturing cost for solar panels and power converters. The main advantage of solar energy is the ability to be used in any place sufficiently sized and perfectly placed photo-voltaic arrays.

Multilevel inverters are one of the most important parts in a photo-voltaic based power generation system. their role in such systems is to synthesize high voltage AC waveforms from different DC voltages generated by PV panels. Usually off-grid PV installations do not require the use of multilevel inverters due to the low voltage generated by the solar panels, instead these installations use two level inverters.

Multilevel inverters are generally used in medium and high power applications such as PV based industrial/commercial installations or High voltage PV generation systems (grid connected).

Figure 1.32 shows multiple multilevel inverter fundamental configuration connected to Photo-voltaic generators, these generators can be arranged in different configurations (series, parallel or both) depending on the desired output power.

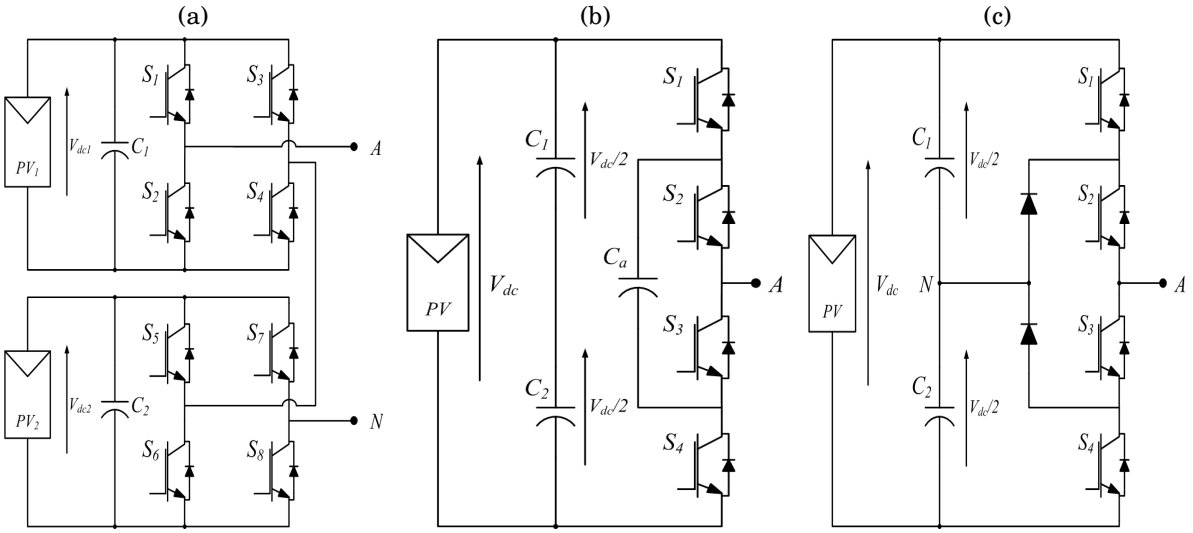

FIGURE 1.32. Multilevel inverter configurations connected to PV generators

Figure 1.33 shows a single phase of a hybrid cascaded multilevel inverter powered by solar panels. The system consists of two conversion systems connected in series. The first converter (up) is DC-AC converter with an auxiliary circuit, in this configuration the converter can generate five voltage levels, whereas the second system is just H-bridge inverter, connecting theses converters together will increase the number of voltage levels. Both converters are connected to DC-DC boost converters to control the voltage produced

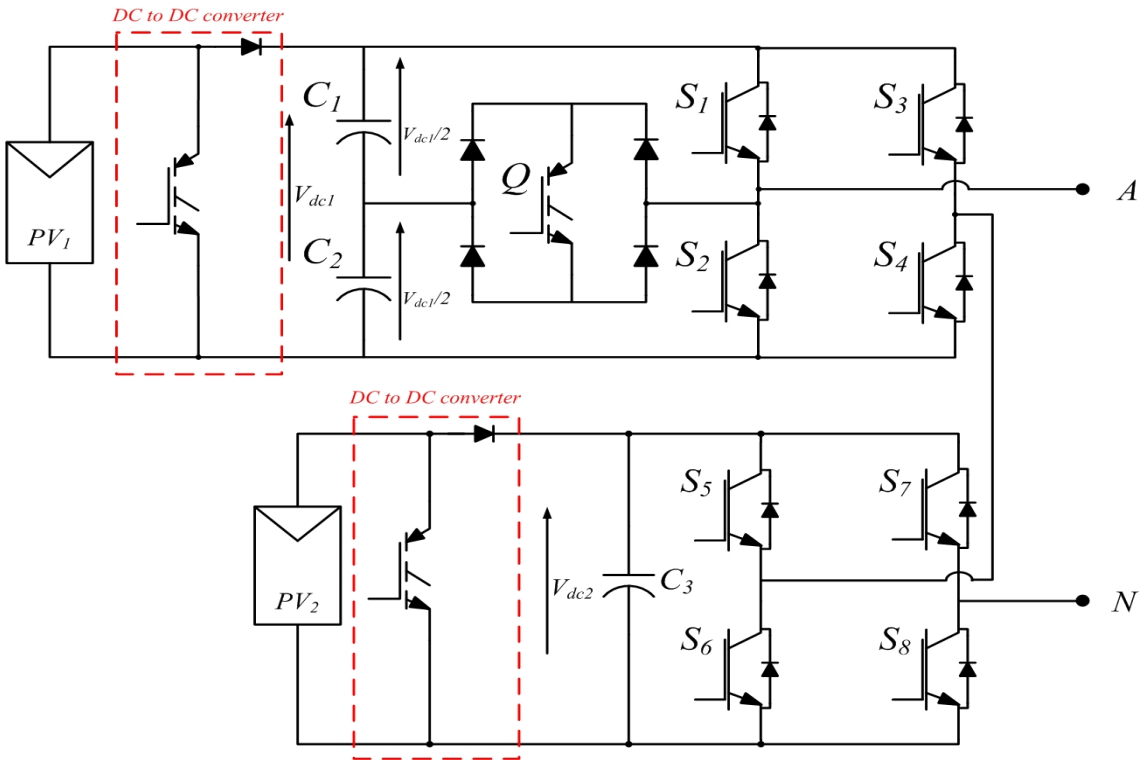

FIGURE 1.33. Cascaded-hybrid multilevel inverter connected to PV generators

by the PV panels. The presented topology is just an example of what can be used for such systems (solar generation systems). Multiple scientists have proposed different multi-level inverter topologies with the aim of optimizing the performance of these inverters and reducing their cost.

1.6.3 HVDC systems

High Voltage Direct Current (HVDC) transmission systems are used to interconnect alternating current systems over a long distance using multilevel converters in back to back configuration. Figure 1.34 shows a typical modular multilevel converter based HVDC transmission system. Conversion stations I and II connected to their respective AC grids through isolation transformers, and their DC system is interconnected through a DC cable several kilometers long. The modular multilevel converter based conversion stations provide high quality output voltage waveforms, which eliminates the need for passive filters[28].

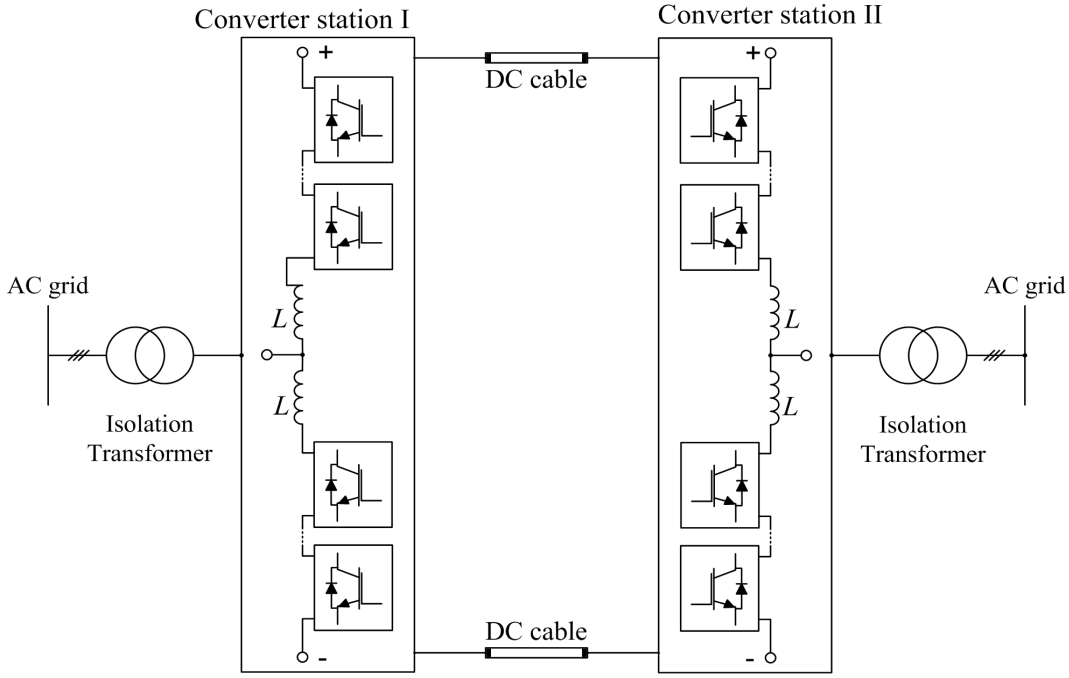

FIGURE 1.34. Modular Multi-Level Converter based HVDC system

1.7 Conlusion

In this chapter, multiple multilevel inverter topologies have been presented, the topologies can be divided into three main categories fundamental, hybrid and reduced device count topologies. The chapter focuses on the reduced device count topologies due to the

various advantages that this category provides such as high reliability, low power loss and simplicity. The chapter also presented some applications of multilevel inverter in order to have better understanding of how these topologies are used in the industry. From structural point of view, the T type inverter configuration is the simplest topology that can generate multiple voltage levels with the least number of switching devices, the number of voltages can be increased by adding more DC sources and bidirectional switches, this can be advantageous in the case of designing a hybrid cascaded inverter. In the next chapter we will introduce the different modulation methods used for controlling multilevel inverters , an adequate modulation strategy will be chosen to drive the proposed multilevel inverter.

CHAPTER 2

CONTROL METHODS FOR MULTILEVEL INVERTERS

The performance of any electrical conversion system depends heavily on the chosen modulation strategy. As demonstrated in figure 2.1, multiple modulation methods have been developed to control multilevel inverters depending on the power range and the nature of the load driven by the converter. Sinusoidal and space vector modulation are two of the most commonly applied control strategies for multilevel DC to AC converters, the main problem with these two techniques is the high switching frequency of the semiconductor devices that leads to high switching losses. A more simple yet efficient modulation method known as selective harmonic elimination can be used for the control of multilevel DC to AC converters; this method is suitable for controlling high power converters due its low switching frequency and better harmonic performance. In this chapter the sine pulse width modulation (SPWM) and the space vector pulse width modulation (SVPWM) methods are briefly reviewed along with a less renowned low switching frequency modulation method called nearest level modulation followed by a detailed analysis on the selective harmonic elimination pulse width modulation.

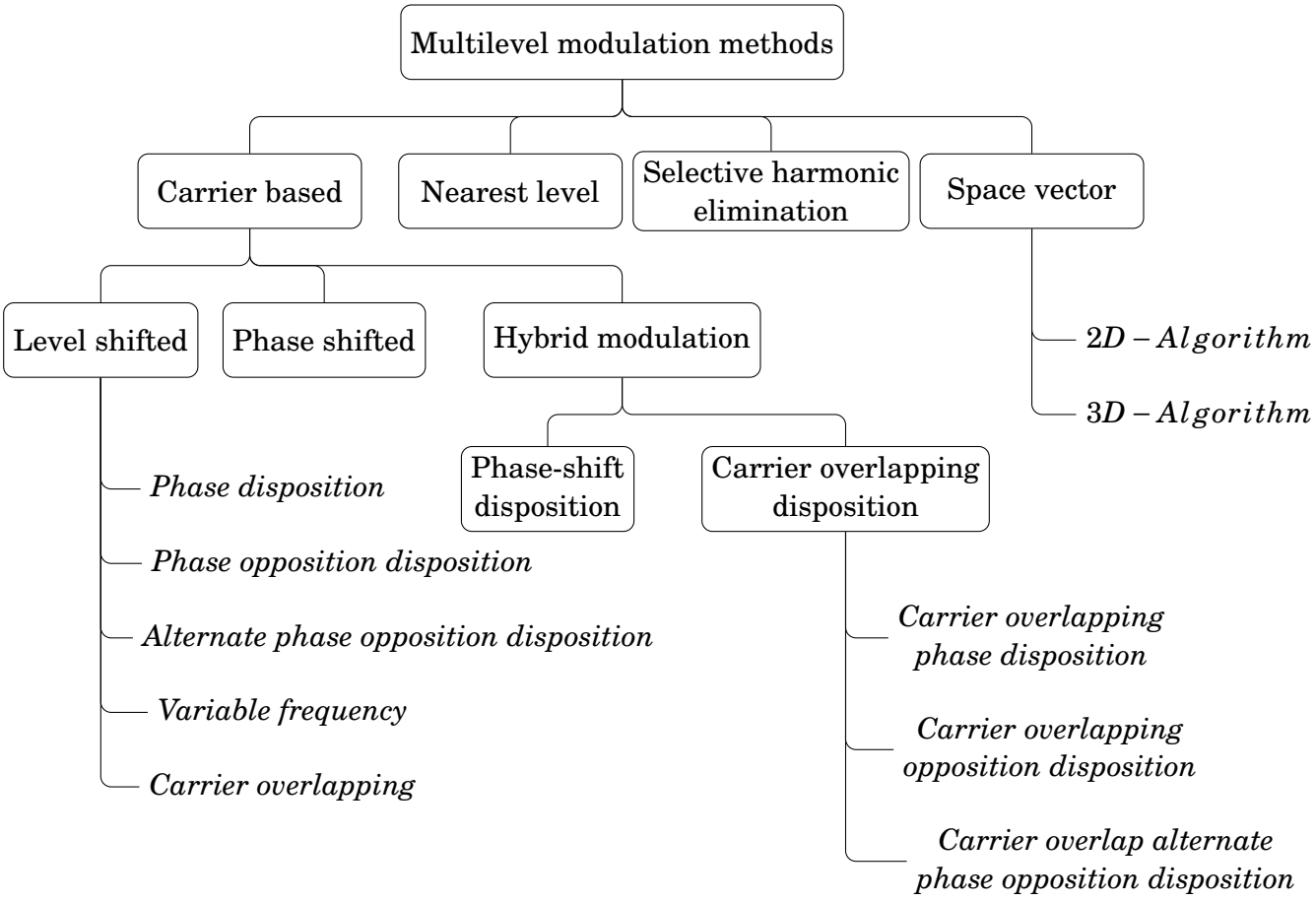

FIGURE 2.1. Widely used modulation methods for multilevel inverters

2.1 Carrier based pulse width modulation

Sinusoidal pulse width modulation (SPWM) is the most used modulation method for the control of multilevel inverter because of its simplicity and good power quality. The main disadvantage of this strategy is the high switching frequency which reduces the lifetime of the switching elements of the multilevel converters.

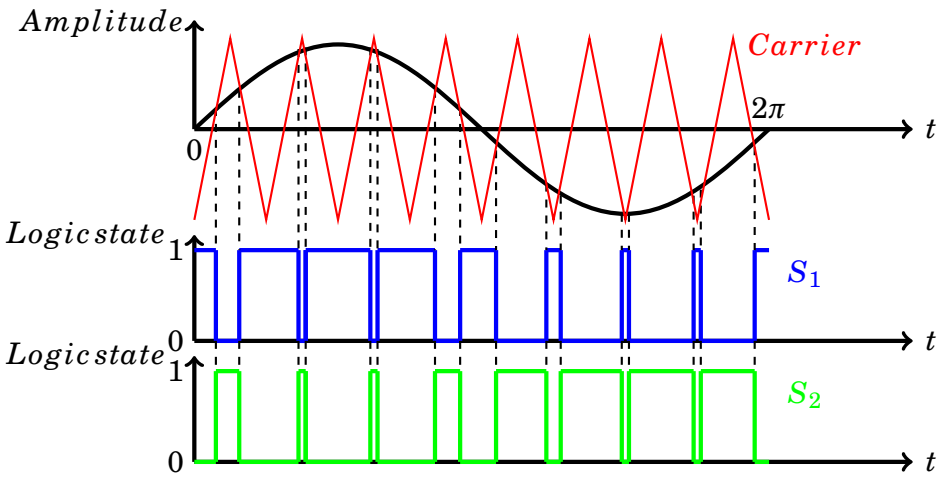

FIGURE 2.2. Sinusoidal PWM method

2.1.1 Level shifted PWM

The basic idea behind the level shifted pulse width modulation (LS-PWM) is to use multiple triangular carrier signals with the same frequency and amplitude shifted at different levels, which are compared to a reference signal as figure 2.5 demonstrates, the interaction between the carriers and the reference signal is used to generate gating signals for the switching elements of the multilevel converter[29, 30].

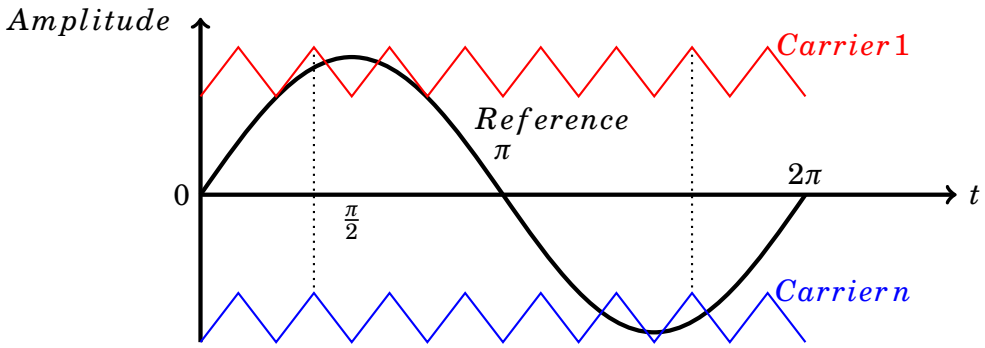

FIGURE 2.3. Generalized level shifted PWM method

Phase disposition, phase opposition disposition and alternate phase opposition disposition are the most common level shifted-PWM techniques used for controlling multilevel inverters. The Phase disposition PWM technique uses multiple triangular carriers with

one reference wave (per phase). In order to generate a waveform with m voltage levels the technique uses $m-1$ carriers of the same amplitude and frequency, figure 2.4(a) shows the phase disposition carrier arrangement for a five level inverter [30].
Figure 2.4(b) demonstrates the arrangement of the carriers for the phase opposition disposition PWM, the carriers above the zero are out of phase to the ones below zero by 180 degrees[30]. The alternate phase opposition disposition (APOD) can be obtained by alternating the phase shift between adjacent carrier as demonstrated in figure 2.4(c)[30].

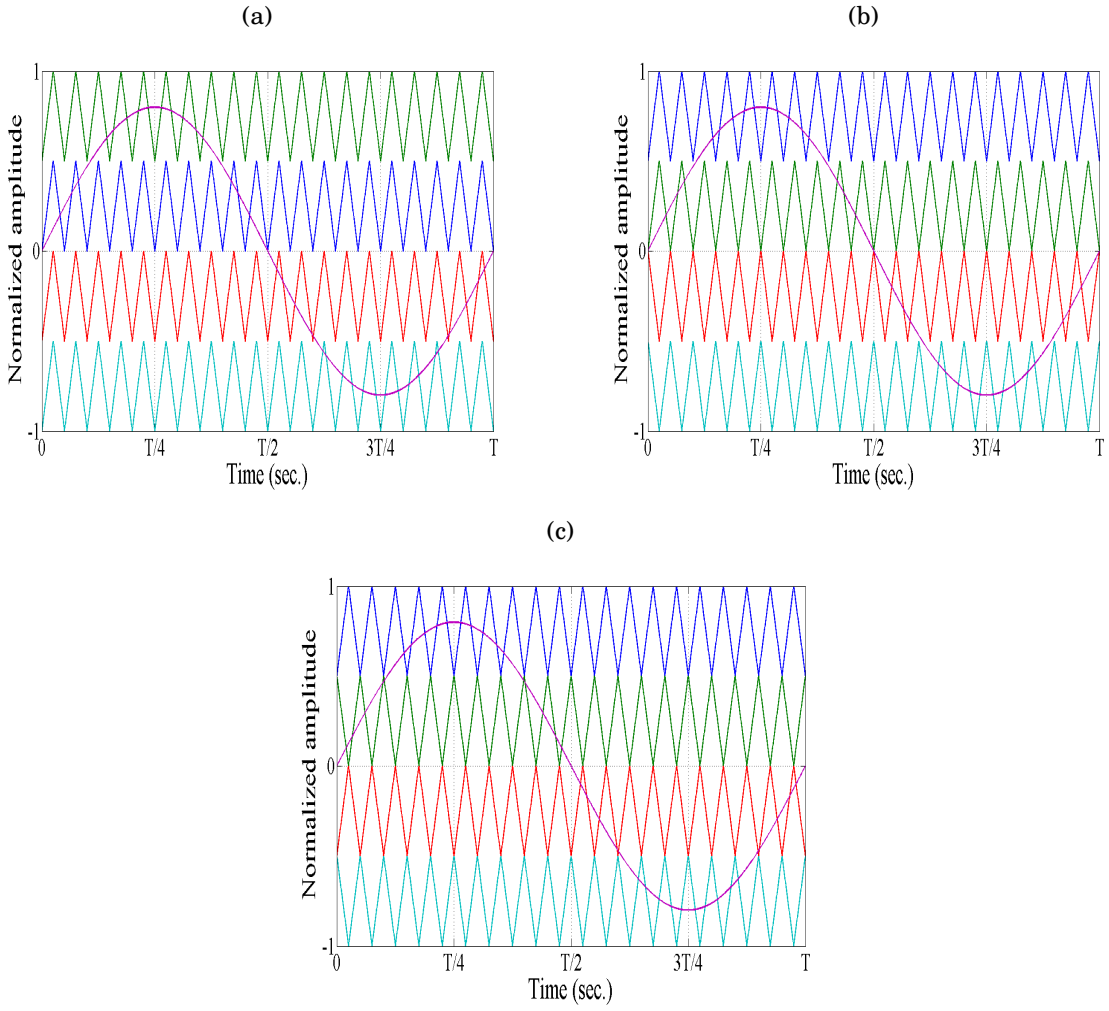

FIGURE 2.4. Level shifted PWM strategies

The level shifted modulation methods are very suitable for neutral point clamped

topology since each carrier can be associated to two complimentary switching elements as figure 2.5 demostrates, the system presented in this figure is a simple analog solution to generate gating signals for three level diode clamped inverter in which the switching states of the four switching elements S_1, S_2, S_3 and S_4 which are determined by comparing a reference signal V_{ref} with a triangular signal (carrier) as mentioned previously.

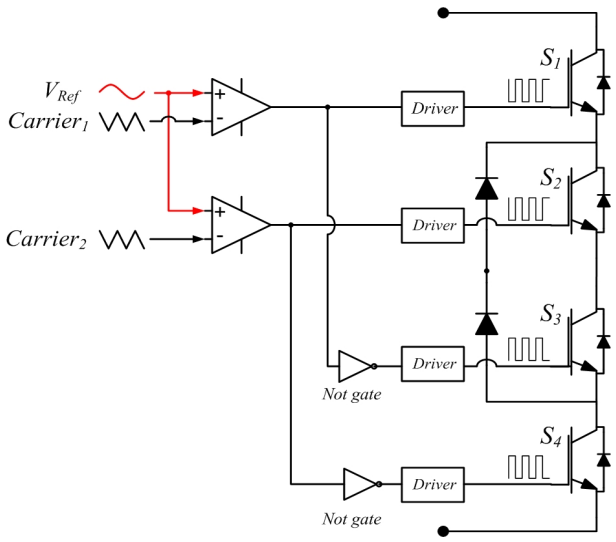

FIGURE 2.5. Analog circuit for generating PWM

Figure 2.6 shows the carrier arrangement for variable frequency PWM which is a modulation strategy derived from PD-PWM, this method was specially created to this method was specially created to equalize the power loss distribution along the converter. Whenever a converter is controlled using phase disposition PWM, the switching elements controlled by the first and last carriers switch states more often than the switching elements controlled by the intermediate carriers. In order to balance the number of transitions, carriers with lower frequency are placed at top and bottom of levels as demonstrated in figure2.6(a)[31, 32].

Figure 2.6(b) shows another case of variable frequency PWM, The intermediate carriers have lower frequency than the carriers situated at top and bottom levels, this arrangement is used to distribute the working load according to the current rating of the

switching elements[32].

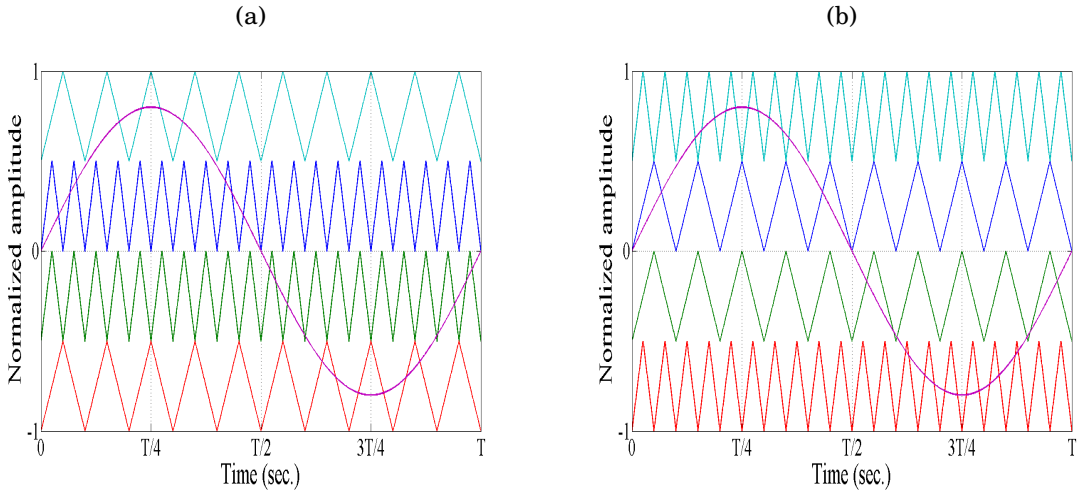

FIGURE 2.6. Variable-frequency carrier PWM

2.1.2 Phase shifted PWM (PS-PWM)

Phase shifted pulse width modulation (PS-PWM) is also a multi carrier modulation method. Similar to the LS-PWM, an m level converter using bipolar phase shifted modulation requires (m-1) carriers, all having the same amplitude, frequency and offset. In this technique the carriers are shifted by $\frac{2\pi}{m-1}$ as demonstrated in figure 2.7[33, 34].

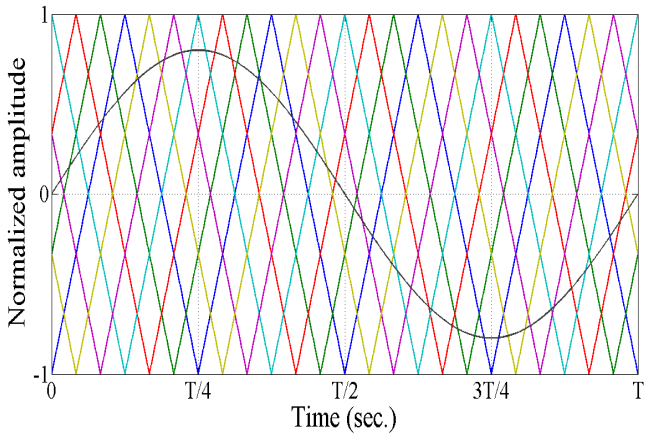

FIGURE 2.7. phase shifted PWM strategy

The phase shifted pulse width modulation method is suitable for flying capacitor and cascaded multilevel inverter based applications [35–38]. The strategy offers better performance than the LS-PWM strategies[].

2.1.3 Hybrid modulation

The hybrid carrier modulation is in part a multi-carrier PWM-based modulation method that is specially conceived for the cascaded and flying capacitor inverters. Phase-shift disposition (PSD) and Carrier overlapping disposition (COD) are two of most widely used hybrid methods.

2.1.3.1 Carrier overlapping disposition

The carrier overlapping disposition strategies (COD-PWM) are a combination of the level shifted carrier overlapping (CO-LSPWM) and other level shifted PWM strategies (PD, POD and APOD). The COD-PWM has multiple variations depending on the arrangement of the carriers; Carrier overlapping-phase disposition (CO-PD), Carrier overlapping-opposition disposition (CO-POD) and Carrier overlap-alternate phase opposition disposition (CO-APOD).

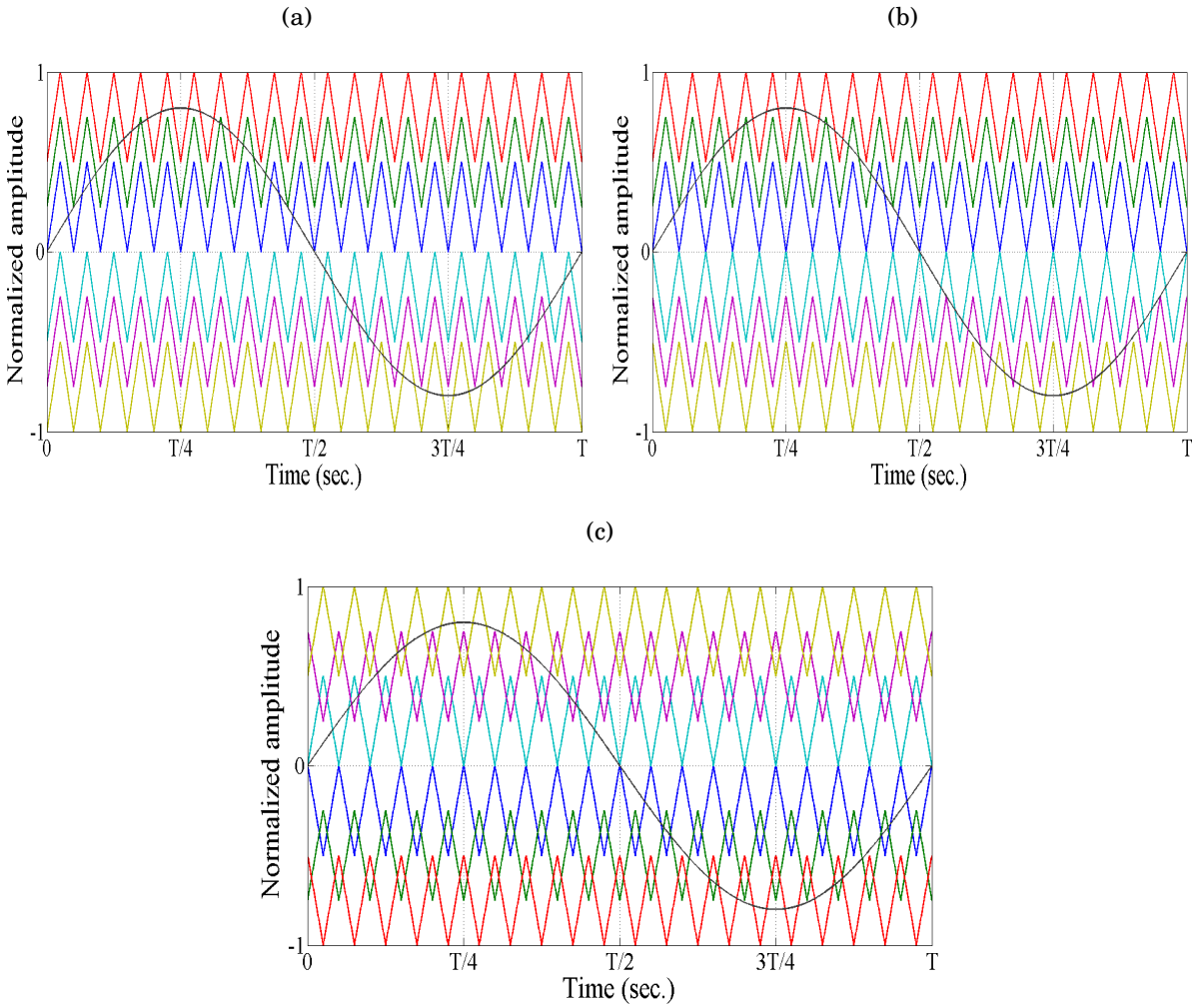

FIGURE 2.8. Carrier overlapping disposition strategies: 2.8(a) carrier overlapping phase disposition PWM, 2.8(b) carrier overlapping phase opposition disposition PWM, 2.8(c) carrier overlapping alternate phase opposition disposition PWM.

The carrier overlapping-phase disposition (CO-PD) method uses $(m-1)$ carriers divided in two groups, the first group located above the zero reference point and the other group is located above the zero reference point, the carriers in this method are in phase. Figure 2.8(a) illustrates the carrier arrangement for this method. Similar to (CO-PD), the Carrier overlapping-opposition disposition (CO-POD) uses $(m-1)$ carriers divided in two groups to control an m-level inverter. However, in this method the second group of carriers is shifted by [pi] as demonstrated in figure2.8(b). Carrier overlap-alternate

phase opposition disposition CO-APOD is a combination of carrier overlapping and level shifted APOD. Similar to the previous COD-PWM methods, this modulation technique uses $(m-1)$ carriers divided in two groups to control an m-level inverter[39, 40]. Each two adjacent carriers are placed in anti-phase as shown in figure 2.8(c).

2.1.3.2 Phase-shift disposition

Phase shifted disposition (PSD-PWM) is a combination of Phase shifted PWM and the Phase disposition modulation method (PD-LSPWM). The algorithm uses two groups of $\frac{m-1}{2}$ carriers shifted by [pi] to drive an m-level converter, the arrangement of the carriers is shown in figure 2.9. The carriers for both groups are shifted by $\frac{4\pi}{m-1}$ [41].

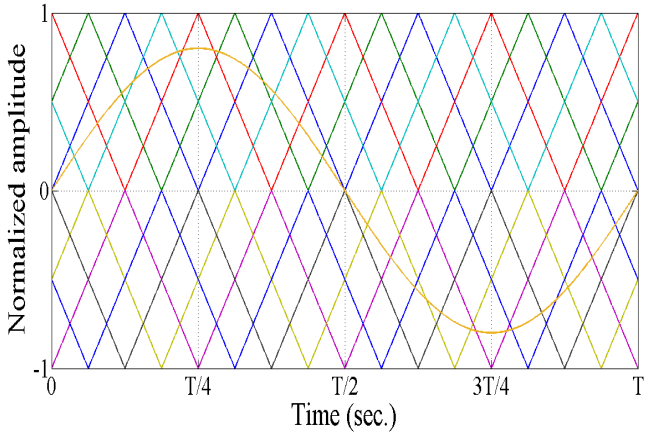

FIGURE 2.9. Phase-shift disposition modulation strategy

The Phase shifted disposition modulation is popularly used to drive Multilevel flying capacitor and neutral point diode clamped converters.

2.2 Nearest level modulation

Nearest level modulation also known as round method, is non-carrier modulation method. In this method the voltage levels are determined by choosing the closest voltage that can be generated by the converter to the reference voltage as demonstrated in figure 2.10.

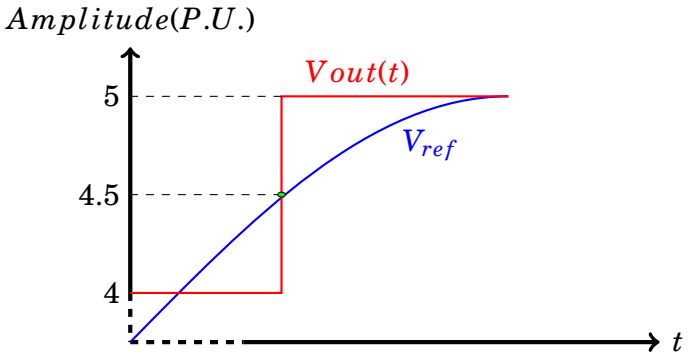

FIGURE 2.10. Nearest level modulation

The output voltage level can be simply computed using this equation.

$$V_a = round\left(V_{ref}.N\right) \tag{2.1}$$

Where V_a is the output voltage level, V_{ref} is the reference voltage and N is the number of attainable voltages. In this modulation method, the modulator is discretized by rounding to the nearest voltage level attainable by the converter. The obtained voltage waveform by this strategy is shown in figure 2.11.

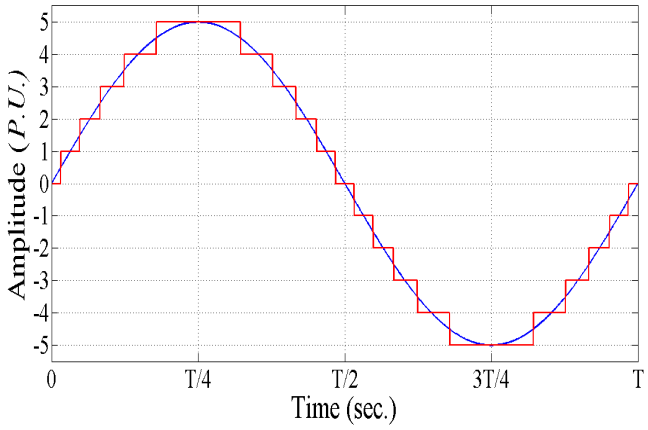

FIGURE 2.11. Nearest level modulation waveform

The NLM method is widely used in high-voltage direct current and other High voltage modular multilevel converter applications[42–44]. Its simplicity makes very easy to be implemented in digital controllers even for a high number of voltage levels[45]. Figure 2.12 shows the block diagram of the NLM method.

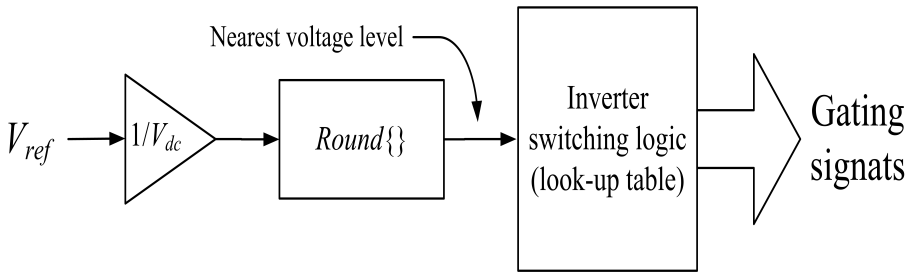

FIGURE 2.12. Nearest level modulation block diagram

2.3 Space vector modulation

Space vector modulation is a well known modulation method. It is generally used to control two level inverters due to its high performance and flexibility. But in the last few years many scientists and engineers proposed the SVPWM as a modulation method for multilevel inverters to improve performance.

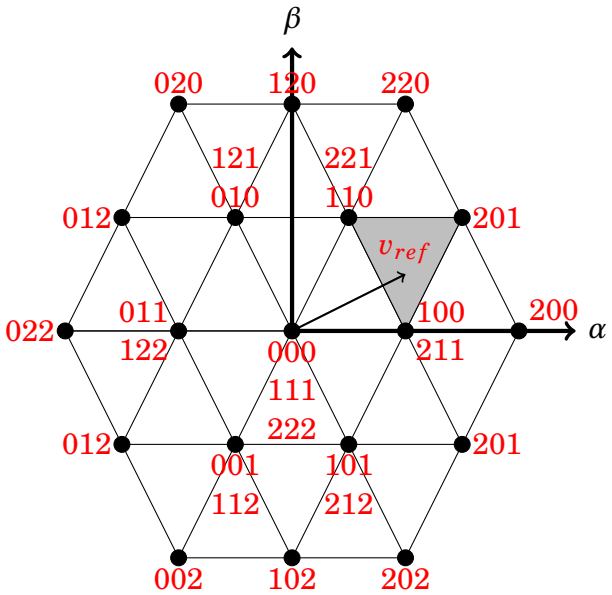

FIGURE 2.13. Control region of a three-level converter α, β coordinates.

Figure2.13 presents a two dimensional representation of the control region of a three level inverter in α-β plane. The idea behind this algorithm is to determine the space

vectors, switching rimes and sequence in which they will be produced in order to approximate in average the reference voltage vector over the modulation period. Multiple SVPWM algorithms have been proposed to control multilevel inverters and each algorithm has its own advantages and drawbacks, but SVPWM algorithms generally perform better than carrier based modulation methods.

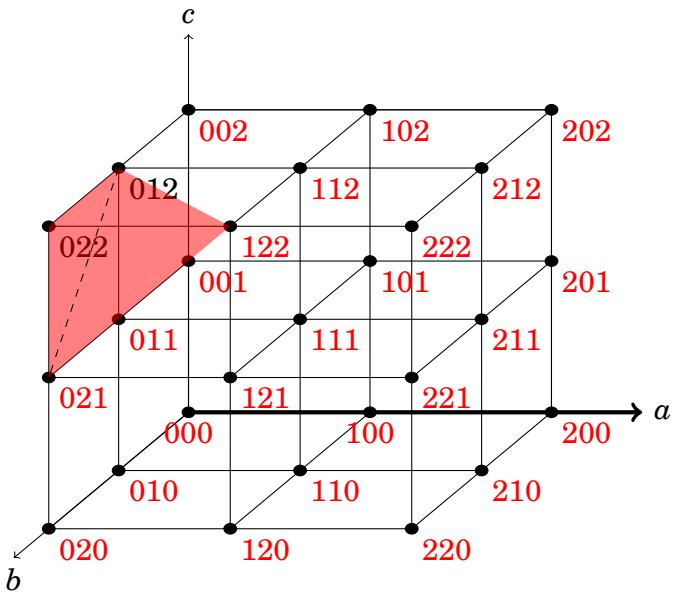

FIGURE 2.14. Control region of a three-level converter abc coordinates.

Most of the SVPWM proposed techniques are based on two dimensional representation of control region as demonstrated previously; these techniques are well suited for topologies where the zero sequence voltage and the zero sequence current are zero.
In some topologies such as four phase converters, the zero sequence voltages and currents are different to zero, therefore the modulation techniques have to consider a three axis plane to perform the modulation without errors. Figure 2.14 shows representation of control region of a three level three phase converter in adc frame. Although SVM modulation methods have better performance than carrier based modulation methods, they are only used to control either low or medium power converters because of the relatively high switching frequency, using these methods to control high power converters may

lead a significant reduction in life span of the switching elements.

2.4 Selective harmonic elimination (SHEPWM)

Sinusoidal and space vector modulation are two of the most commonly applied control strategies for multilevel DC to AC converters, the main problem with these two techniques is the high switching frequency of the semiconductor devices that leads to high switching losses. A more simple yet efficient modulation method known as selective harmonic elimination can be used for the control of multilevel DC to AC converters [46–51]; the method was introduced for the first time in 1973 by Patel and Hoft in [52]. The method was used to eliminate harmonics in single and three phase Thyristor controlled inverters. The method provides a lot of advantages such as eliminating low rank harmonics and operating the switching devices at a low frequency which leads to increasing the lifetime of switching components[53, 54].

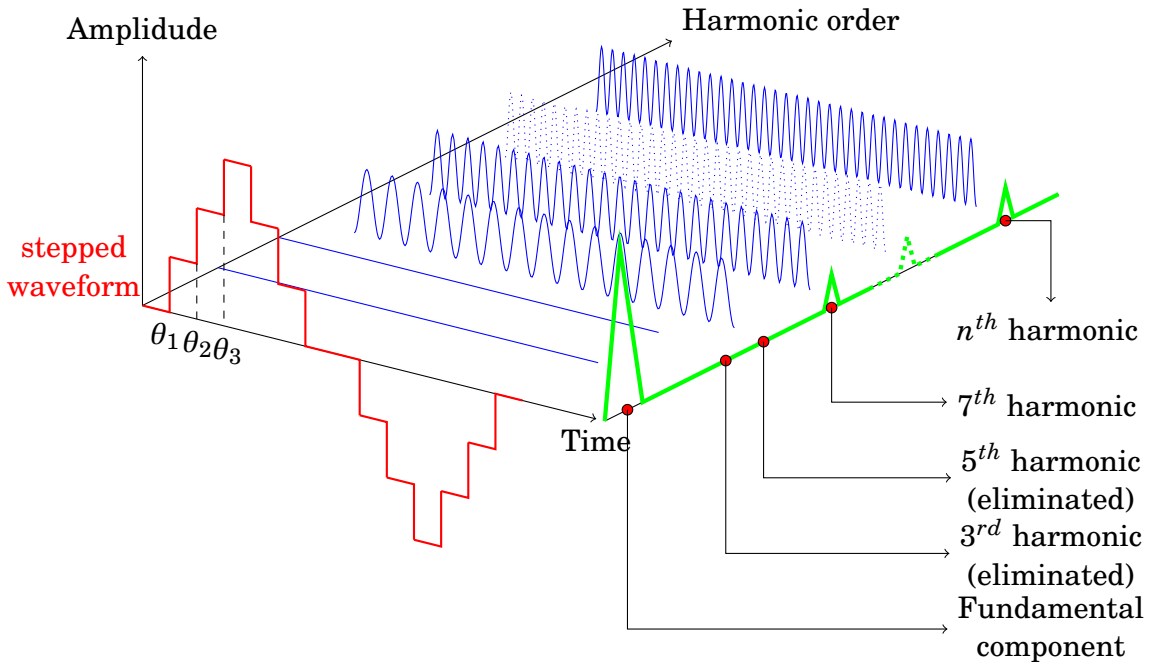

FIGURE 2.15. Selective harmonic elimination

The selective harmonic elimination pulse width modulation strategy is based on the Fourier series decomposition of the waveform generated by a power converter, as demonstrated in figure 2.15. For a uniform stepped waveform as the one demonstrated in figure 2.16, it can be expressed in this form:

$$v_{out}(\theta) = A_0 + \sum_{n=1}^{\infty} A_n \; cos(n\theta) + B_n \; sin(n\theta) \tag{2.2}$$

with

$$A_0 = \frac{1}{2\pi}\int_0^{2\pi} f(t)dt \tag{2.3}$$

$$A_n = \frac{1}{\pi}\int_0^{2\pi} f(t)\sin n\omega t dt \tag{2.4}$$

$$B_n = \frac{1}{\pi}\int_0^{2\pi} f(t)\cos n\omega t dt \tag{2.5}$$

Where A_0 is the DC component, A_n is the sine Fourier coefficient, B_n is the cosine Fourier coefficient. Since the generated waveform has no DC component (average value) and characterized by quarter wave and half wave symmetry, therefore $A_0 = 0$ and the expression presented in equation (2.2) is reduced to:

$$V(\theta_i) = \sum_{n=1,3,5,\ldots}^{\infty} \left[\frac{4V_{dc}}{n\pi}\sum_{i=1}^{p}\cos(n\theta_i)\right]\sin(n\theta_i) \tag{2.6}$$

For a uniform stepped waveform with shifting polarity, the voltage waveform can be expressed as follows[55, 56]:

$$V(\theta_i) = \sum_{n=1,3,5,\ldots}^{\infty} \left[\frac{4V_{dc}}{n\pi}\sum_{i=1}^{p}(k)\cos(n\theta_i)\right]\sin(n\theta_i) \tag{2.7}$$

The value of the parameter k defines each transition of the waveform where:

$$k \rightarrow \begin{cases} 1 & for\ the\ rising\ edge \\ -1 & for\ the\ falling\ edge \end{cases} \tag{2.8}$$

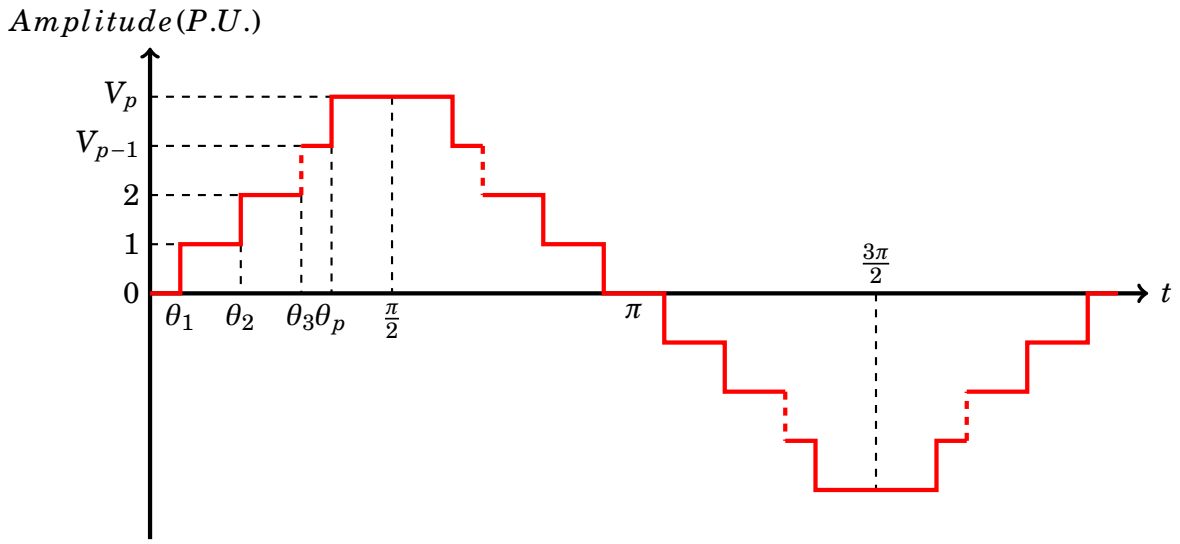

FIGURE 2.16. Uniform stepped waveform

To ensure a quarter waveform symmetrical and physically correct waveform the switching angles within the quarter waveform must respect the following constraint:

$$0 < \theta_1 < \theta_2 < \theta_3 < \ldots < \theta_p < \frac{\pi}{2} \tag{2.9}$$

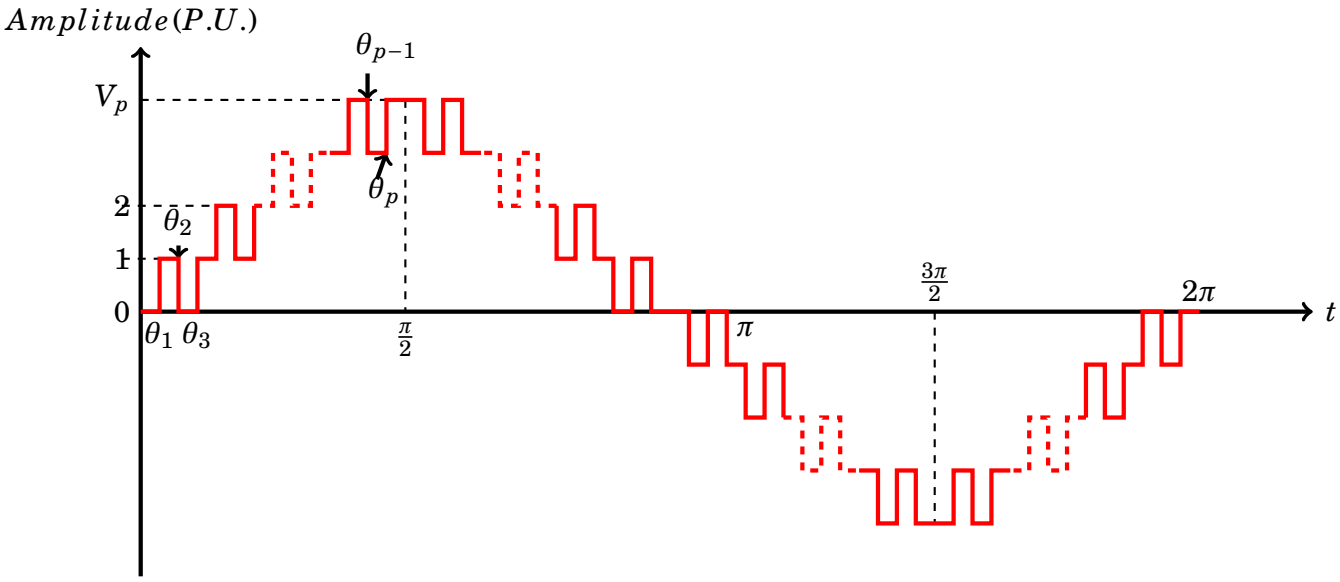

FIGURE 2.17. Generalized stepped waveform

For n level inverter, it is possible to eliminate $((n-1)/2)-1$ undesired harmonics while maintaining the desired value of the fundamental voltage. From equation (2.6), the magnitudes of the Fourier coefficients when normalized with the respect to V_{dc} , can be expressed as follows:

$$\begin{cases} H_1 = \cos(\theta_1) + \cos(\theta_2) + \ldots + \cos\left(\theta_p\right) - m = 0 \\ H_2 = \cos(3\theta_1) + \cos(3\theta_2) + \ldots + \cos\left(3\theta_p\right) = 0 \\ H_3 = \cos(5\theta_1) + \cos(5\theta_2) + \ldots + \cos\left(5\theta_p\right) = 0 \\ \vdots \\ H_N = \cos(n\theta_1) + \cos(n\theta_2) + \ldots + \cos\left(n\theta_p\right) = 0 \end{cases} \tag{2.10}$$

In order to eliminate the undesired harmonics the set of transcendental equations (2.6) must be solved for a given value of m, where $m = (((N-1)/2)r/4)$, r is the modulation index.

Solving the system of non linear equation can be done by either using analysis or optimization methods as it will be demonstrated in the next chapter. An objective function is an essential element in any optimization process. The objective function must be formulated in such a way that allows us to eliminate the low order harmonics and maintain the fundamental component at a desired value; therefore it is chosen to be as follows:

$$F(\theta) = F\left(\theta_1 \ldots \theta_p\right) = \left(\sum_{i=1}^{p} \cos(\theta_i) - \frac{p\pi}{4} r\right)^2 + \sum_{n=3,5}^{2p-1} \sum_{i=1}^{p} \cos(n\theta_i) \tag{2.11}$$

The objective function can be formulated depending on the targeted objective.

Changing the value of r can have a significant effect on the power delivered to the load (fundamental component). Figures 2.18 and 2.19 show the impact of varying the value of r.The figures also demonstrate the ability of eliminating independently any harmonic using the SHEPWM strategy. The tests were carried out on a mathematical model and a laboratory prototype of a five level inverter.

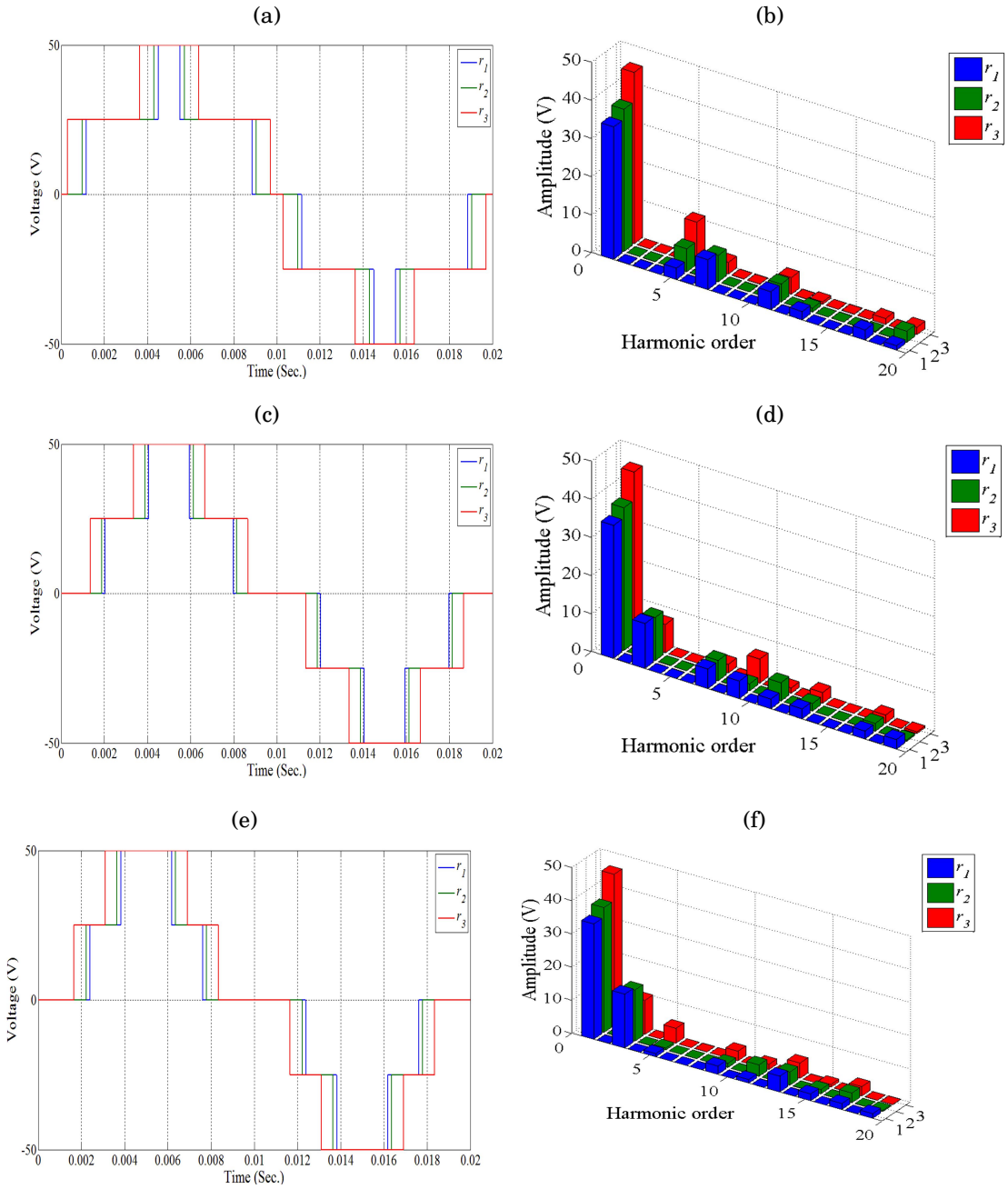

FIGURE 2.18. Output voltage and the corresponding FFT analysis in the case of eliminating 3rd, 5th and the 7th harmonic

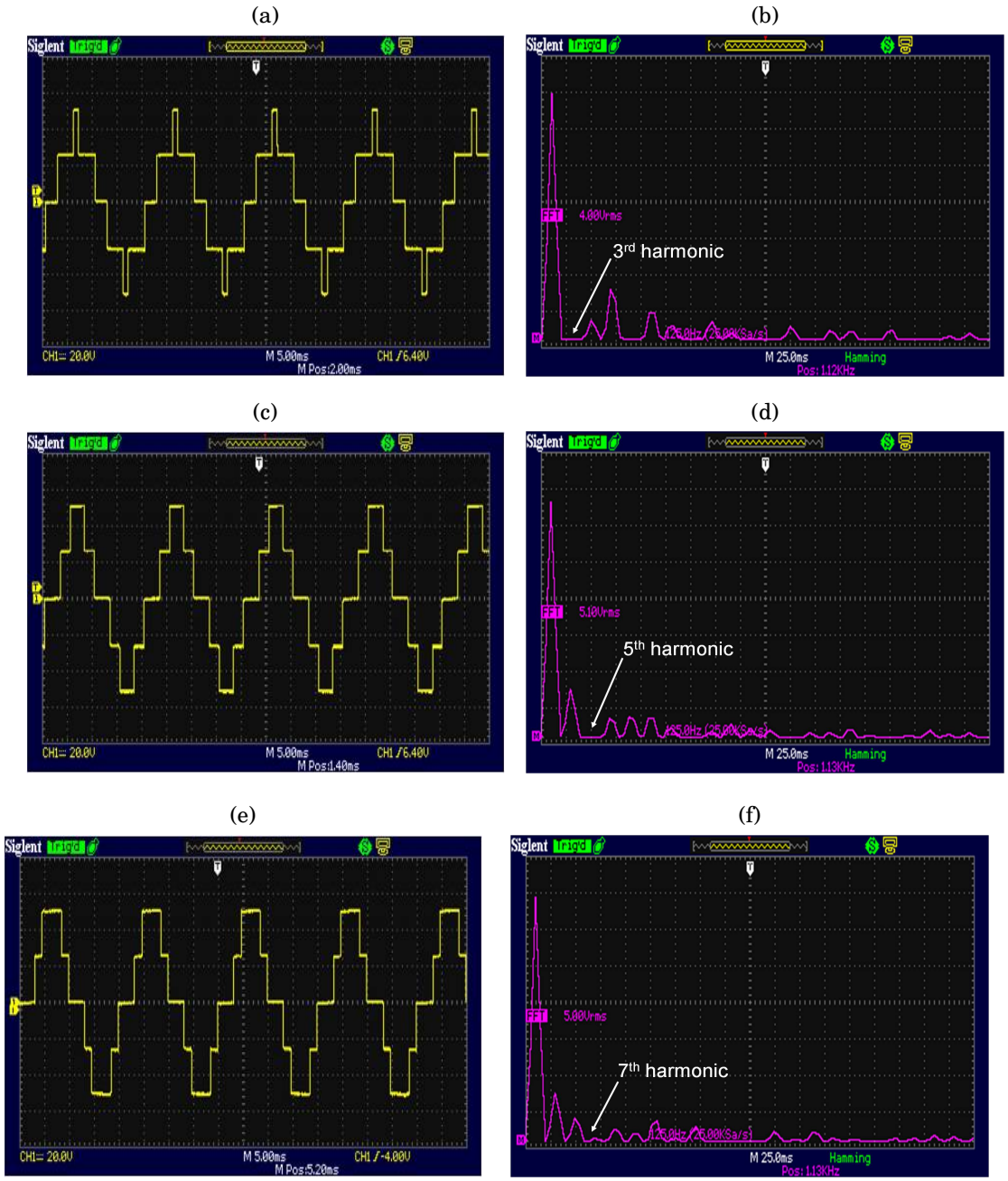

FIGURE 2.19. Experimental Output voltage and the corresponding FFT analysis in the case of eliminating 3rd, 5th and the 7th harmonic

The left side of figures 2.18 and 2.19 show the generated waveforms in the case of eliminating the third, fifth and the seventh harmonics respectively, and for different modulation indices r where $r_1 = 0.7$, $r_2 = 0.85$ and $r_3 = 0.9$, whereas the left side of the

same figures show the FFT analysis of the generated waveforms for the above mentioned cases and also for different values of r. It can be noticed from the voltage waveforms that by decreasing the modulation index, the switching angles will have higher values and this will lead to a decrease in the amplitude of the fundamental component this effect can be clearly observed in the FFT analysis figures. And also it can be clearly seen from the FFT analysis that the undesired harmonics were successfully eliminated in each case, for example in figure 2.19(b) the third harmonic was eliminated while the fifth harmonic remained untouched, whereas in figure 2.19(d) the fifth harmonic was eliminated while the third and the seventh harmonics remained untouched.

2.5 Dead time Insertion

The half bridge as a basic unit uses two switching elements connected in series across the voltage source. The switching elements must be controlled in a complementary manner in order to avoid short-circuit. Nevertheless there is always a possibility of unexpected short circuit, due to the switching characteristics of the semiconductor devices. For instance figure 2.20 shows the switching characteristics of an IGBT, it can be clearly seen from the figure that the turn-off time is longer than the turn-on time[57, 58]. Therefore, when the complementary gating signals are given to the switching devices at the same time, a short circuit is likely to happen; because one of the switching elements is being driven *ON* while the other is may be still conducting[59].

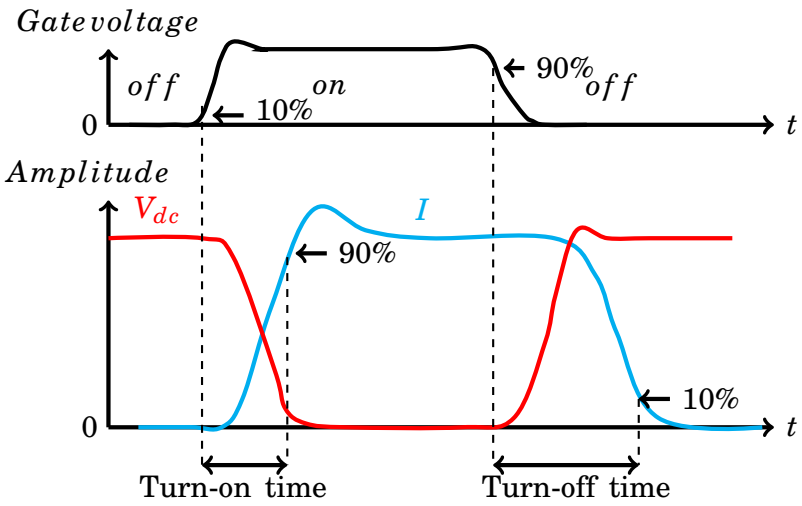

FIGURE 2.20. IGBT switching characteristics

In order to avoid short-circuit of the DC-link, a time delay is inserted between the gating signals as demonstrated in figure 2.21. This delay is known as dead time or blanking time[60].

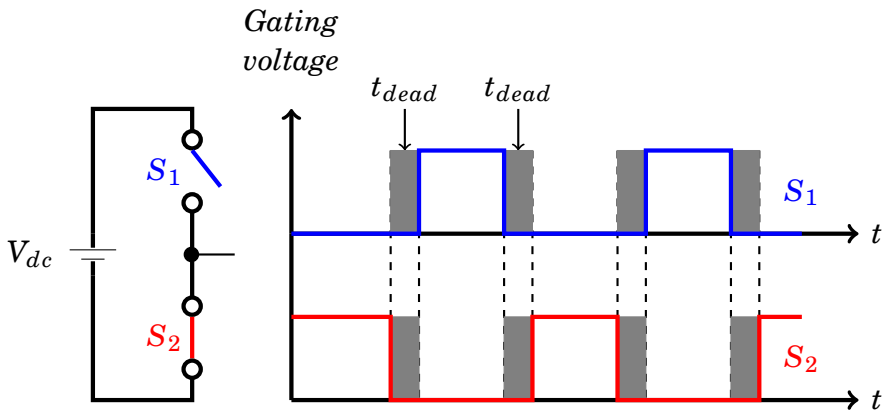

FIGURE 2.21. Dead time insertion.

Although the dead time, ensures safe operation of the converter, it causes serious distortion in the output voltages[61].

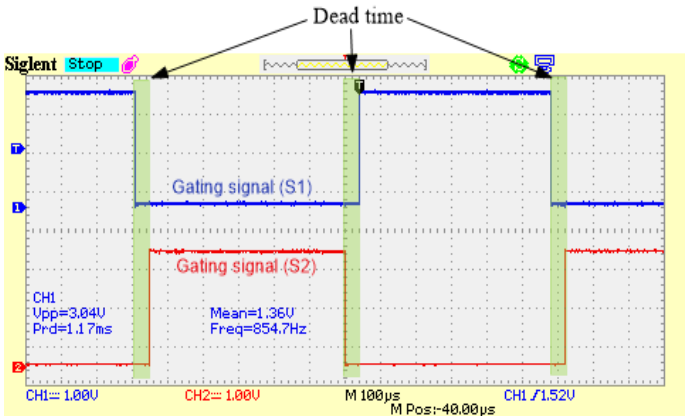

FIGURE 2.22. Gating signals with dead time insertion generated using a microcontroller

2.6 Conclusion

In this chapter we presented some of the widely used modulation methods used to control multilevel inverters. Our aim is to find a proper modulation method suited to control high voltage high power multilevel inverter. Carrier based and space vector modulation methods are known for their high switching frequency, these methods are usually used to control systems with fast dynamic. Using these methods to control a high voltage converter will lead to a significant reduction of the switching elements life span or even cause instant damage to them which leaves us with two options, using the nearest level or the selective harmonic elimination strategy. The nearest level strategy is the simplest modulation strategy used to control multilevel inverters since it does not require a lot of mathematical functions to use it; this means it can be easily implemented on a low cost microprocessor. The main disadvantage of this strategy is the high number of harmonics, for high voltage system this can have devastating effects on the load and the converter alike. This leaves us with only option: using selective harmonic elimination strategy. As shown in the chapter, the selective harmonic elimination is low frequency modulation strategy, as its name suggests, it allows us to eliminate undesired harmonics while controlling our converters at low switching frequency. The main disadvantage of this strategy is that it requires solving a system of non linear equations in order to determine

optimal switching angles. This can be done either by using numerical or optimization methods. The next chapter presents several methods that can be used to solve this problem.

CHAPTER 3

APPLICATION OF ADVANCED CONTROL METHODS ON MULTILEVEL INVERTERS

Several numerical methods have been used to compute the optimal switching angles such as the theory of resultants and Newton-Raphson (N-R), but these methods are difficult to use especially when it comes to solving large number of equations. The (N-R) method requires an initial guess of the switching angles in such a way that they are close to the optimal values. Guessing the initial solutions of a set of nonlinear equations is extremely difficult especially for a large number of variables (switching angles). Another approach to solve the optimal switching problem is by using optimization algorithms, where the equations of SHEPWM are presented in a cost function that can be optimized. Multiple optimization methods were used for SHEPWM problem such as PSO [3] and genetic algorithms [5]. These methods allow the determination of the switching angles without an initial guess.

3.1 Application of optimization methods:

Newton-Raphson (NR) method is one of the most widely used and also one the fastest iterative methods for root-finding.

In the optimal switching problem(SHE) the NR method is used to solve the system of transcendental equations expressed in (2.10) to obtain the optimal switching angles. The system can be written in following form:

$$F(\theta) = B \tag{3.1}$$

Where:

$$F(\theta) = \begin{bmatrix} \cos(\theta_1) & \cos(\theta_2) & \cos(\theta_3) \\ \cos(3\theta_1) & \cos(3\theta_2) & \cos(3\theta_3) \\ \cos(5\theta_1) & \cos(5\theta_2) & \cos(5\theta_3) \end{bmatrix} \tag{3.2}$$

And

$$B = \begin{bmatrix} rn \\ 0 \\ 0 \end{bmatrix} \tag{3.3}$$

Which represents the desired amplitudes for the fundamental component, 3^{rd} and 5^{th} harmonic respectively.

In order to solve this system of equations of any value of r the following steps must be achieved:

- guess the initial values of the optimal angles θ^0 where:

$$\theta^0 = \begin{bmatrix} \theta_1^0 \\ \theta_2^0 \\ \theta_3^0 \end{bmatrix} \tag{3.4}$$

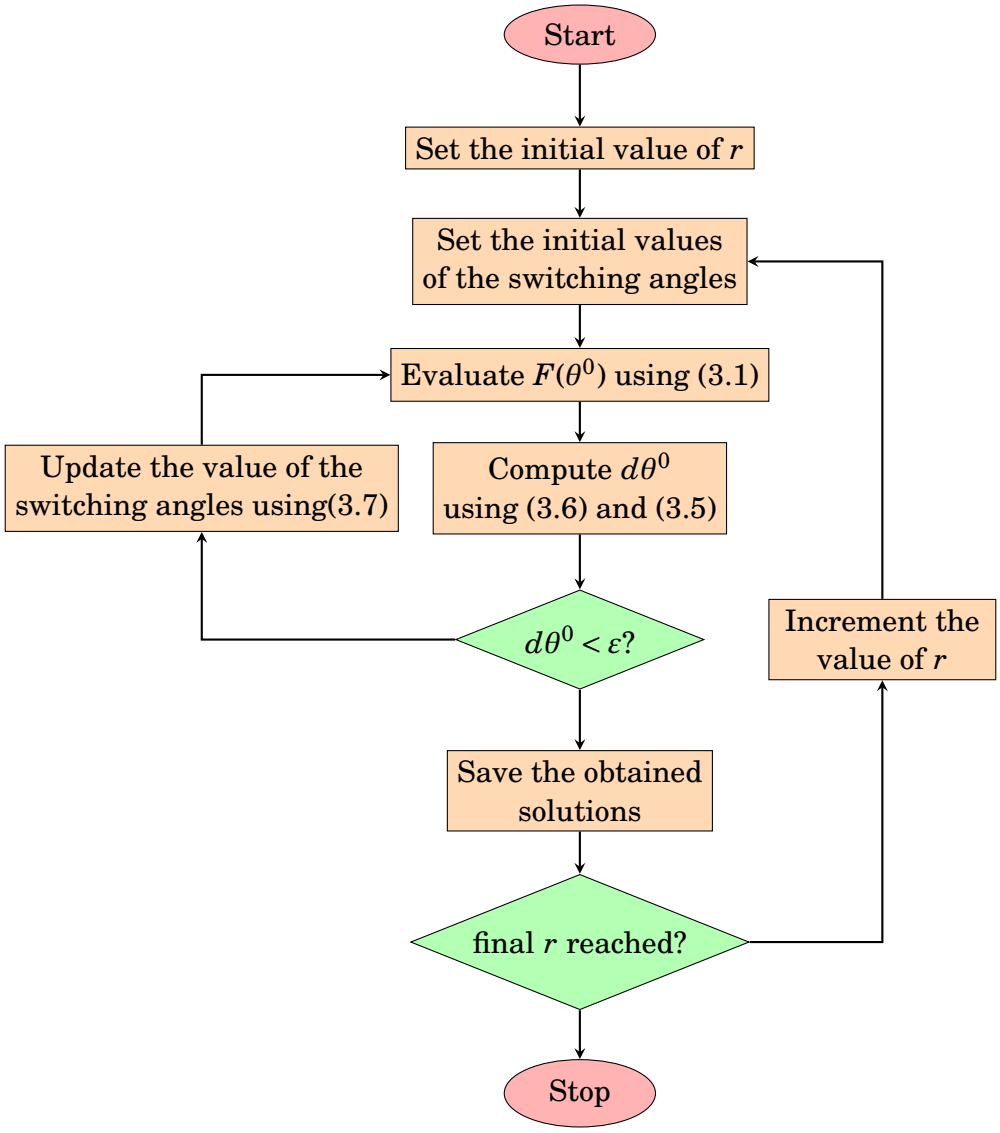

FIGURE 3.1. Flowchart of the NR algorithm..

- Evaluate $F(\theta)$ and $B(r)$ using (5) and (6) then compute the jacobian matrix $J(\theta)$

  Where :

$$J(\theta) = \begin{bmatrix} -\sin(\theta_1) - \sin(\theta_2) - \sin(\theta_3) \\ -3\sin(3\theta_1) - 3\sin(3\theta_2) - 3\sin(3\theta_3) \\ -5\sin(5\theta_1) - 5\sin(5\theta_2) - 5\sin(5\theta_3) \end{bmatrix} \tag{3.5}$$

- Compute $d\theta$ using the following relation :

$$d\theta = INV\,[J(\theta)](B - F) \tag{3.6}$$

- Update the values of θ using the following relation:

$$\theta^{k+1} = \theta^k + d\theta^k \tag{3.7}$$

  Where k is the current iteration.

- Repeat steps 2 (Evaluation) to 4 (update) for a number of iterations (k) to reach an acceptable error value $d\theta$.

Figure 3.1 presents the computational process using NR algorithm for different values of r.

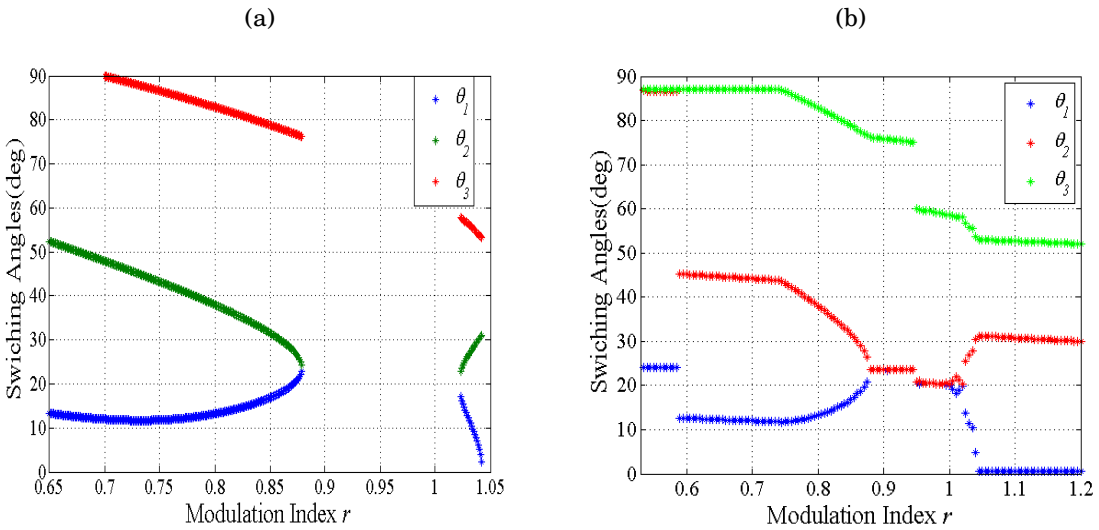

FIGURE 3.2. Switching angles obtained by using NR and DE algorithm.

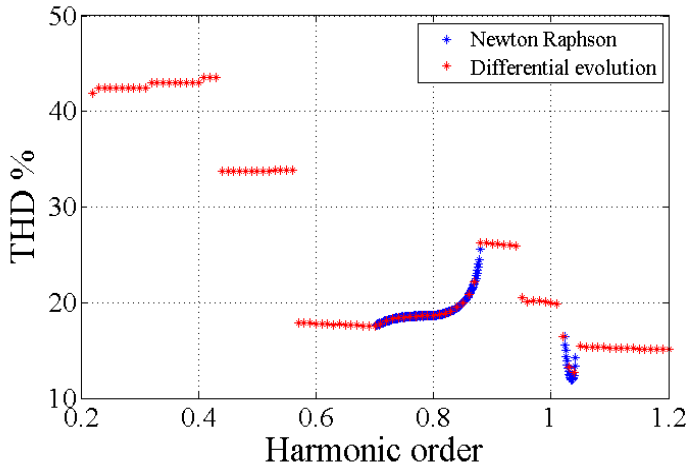

FIGURE 3.3. THD NR and DE algorithm.

3.1.1 Particle swarm optimization

Particle swarm optimization is a population-based search method based on the simulation of the social behavior of birds [62, 63], the algorithm was first introduced by James Kennedy and Russell Eberhart in 1995 [64, 65]. The proposed algorithm has drawn much attention from the scientific community and been successfully applied in many complex optimization problems and industrial applications [66–71] .For the optimal switching problem each particle of the population is composed of switching angles per quarter waveform. To begin the search operation, the switching angles are generated randomly is such way that satisfies the constraint expressed in (2.9) for the chosen number of population. Using the generated values, individual harmonics are calculated, which represents the fitness of a search point. The best set of switching angles among the population at certain iteration is called present best solution (pbest). The best solution up to present iteration is called the global best solution (gbest) for the variables θ_1 through θ_{10}. At each iteration, new search points are created from the current points and the information regarding the pbest and gbest solutions using the following equations[

$$v_i^{k+1} = wv_i^k + c_1 rand(pbest_i^k - x_i^k) + c_2 rand(gbest_i^k - x_i^k) \tag{3.8}$$

and

$$x_i^{k+1} = x_i^k + v_i^{k+1} \tag{3.9}$$

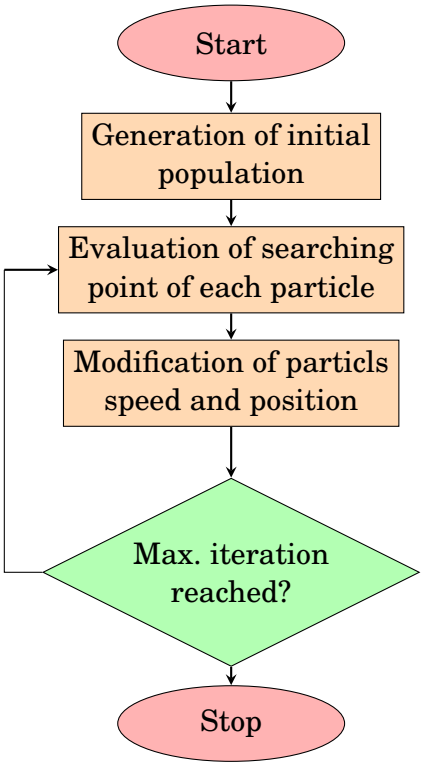

FIGURE 3.4. particle swarm optimization (PSO) flowchart.

where v_i is the velocity, w is the weight, $rand$ is a random number between 0 and 1, c_1 and c_2 are the constriction factors, and k is the iteration number.

3.1.2 Genetic algorithms and differential evolution

3.1.2.1 Genetic algorithms

Genetic algorithm is a stochastic global search algorithm that can solve almost all optimization problems by imitating biological evolution in nature [72], it was first proposed by John Holland in 1975 [73]. GA has been successfully applied over the years to a wide range of probelms of significant complexity [74–78]. The structure of a simple

genetic algorithm consists mainly of three operators: a selection operator, a crossover operator that acts on a population of strings to perform the required reproduction and recombination, and a mutation operator [79, 80]. The process of a basic genetic algorithm consists of four main steps.

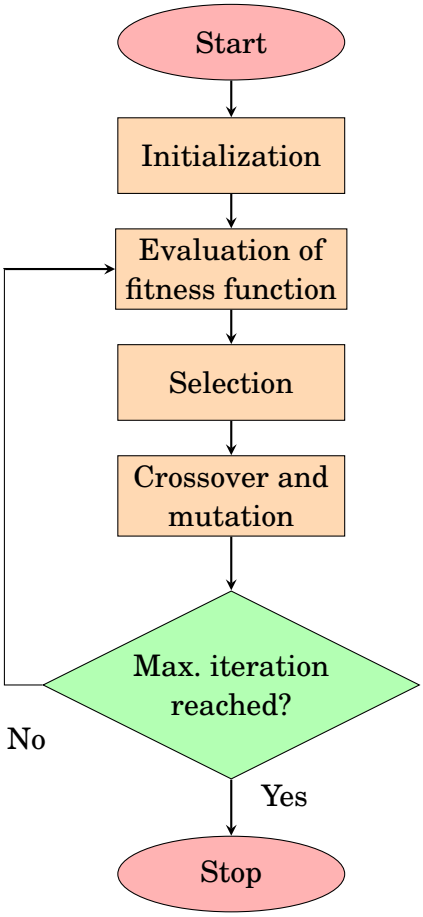

FIGURE 3.5. Genetic algorithm (GA) flowchart.

Initialization: For any genetic algorithm it is necessary to initialize the population. One of the most used methods is to randomly generate solutions (chromosomes)for the entire population. Population size depends on the nature of the optimization problem.

Evaluation of fitness function: In order to test the efficiency of the generated solutions, a fitness function is used as a measure. In the case of the optimal switching

problem for n-level inverter, Equation (2.11) is defined as the objective function.

Selection: In this phase, parents are appointed based on selection rules to generate offspring chromosomes (solutions). The selected parents are the main contributors to form the next generation, where the fittest individuals are likely to survive and the less fit are eliminated.

Crossover and mutation: In this phase, new individuals are generated by the method of intersection; this phase is considered as a very important and a powerful genetic operator. Mutation is performed by altering genes and, finally, the new generated population is ready for another cycle of the genetic algorithm.The genetic algorithm runs a certain number of iterations as required by the user. Figure 3.5 shows the flowchart of a basic genetic algorithm.

3.1.2.2 Differential evolution

The differential evolution (DE) is one of the most powerful optimization algorithms. Since its introduction in 1997 [81, 82], the algorithm has drawn the attention of many scientists over the world and has been applied in different optimization applications [83–86], resulting in multiple variants derived from the original basic algorithm, with improved performance. The DE is a simple yet powerful algorithm; it is composed of three main operations mutation, crossover and selection [87, 88]. The algorithm uses the difference of solution vectors to create new candidate solutions using the above-mentioned operators.

The differential evolution algorithm (DE) is an optimization method is composed of three main steps initialization, mutation and crossover. The general structure of a DE program is shown in figure 3.6. The algorithm perturbs the population of vectors by employing the mutation, whereas its diversity is controlled by the cross-over process [89].

In the case of SHPWM, differential evolution algorithm is used as an optimization tool to perform a random search for the global minima, which is forcing the objective function (2.11) towards an allowable error value.

The optimization process starts by initializing the necessary parameters of the algorithm, such as the population size (NP), crossover probability (CP), upper and lower bounds (θ_{min} and θ_{max}) and the maximum number of iterations. It should be noted that the boundaries must satisfy equation (2.9). The next step is to randomly generate an initial population of switching angles in this process the algorithm creates

$$\theta_{ij}^{(0)} = \theta_{\min ij} + rand_i \left(\theta_{maxj} - \theta_{minj}\right) \tag{3.10}$$

With $i = 1,2,\ldots,NP$ and $j = 1,2,\ldots,N$

Where $\theta_{ij}^{(0)}$ is the initial population, i presents the population size, j is the number of decision variables which represents the number of switching angles. After the initialization process, the generated population is evaluated, the evaluation of the fitness of each individual is carried out by using (2.11).

The mutation process creates a mutant v_{ij} vector based on the initial population; this process is described by the following expression

$$v_{ij} = X_{r1} + F(X_{r2} - X_{r3}) \tag{3.11}$$

X_{r1}, X_{r2} and X_{r3} are vectors randomly sampled from the generated population, $\mathrm{X_r} = [\theta_{\mathrm{i1}}, \theta_{\mathrm{i2}}, \ldots, \theta_{\mathrm{iN}}]$ the indices $r1, r2$ and $r3$ are integers randomly chosen from the range $[1NP]$, they are also chosen to be different from the index i, the parameter F is the mutation constant which controls the amplification of the differential variation $(X_{r2} - X_{r3})$, the value of this parameter is randomly generated from the range [01], it should be noted that multiple mutation methods were reported in[90].

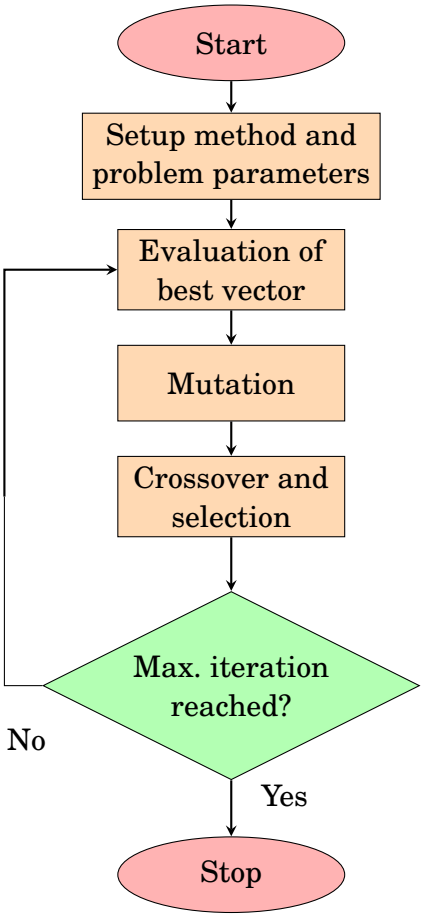

FIGURE 3.6. Differential evolution (DE) flowchart.

To improve the diversity of the population, the crossover operation comes into play, after generating the mutant vector v_{ij} through mutation, this operation assures the production of fitter individuals, the result of this process is a vector u obtained by mixing the components of v_{ij} and X_i the process can be expressed as:

$$u = \begin{cases} v_{ij} \; if \; rand \leq CP \; or \; j = j_{rand} \\ Xi \qquad\qquad\qquad\qquad otherwise \end{cases} \tag{3.12}$$

Where $rand$ is a random number in the range of [01], CP is the crossover probability constant, it controls the diversity of the population and it has a value between 0 and 1 [91], j_{rand} is randomly chosen index. Once the crossover process is completed, the selection process comes into play to decide whether the u_i or $X_i$vector survives for the

next generation, this process is carried out to choose the fittest individual. The selection process can be expressed mathematically as:

$$X_i^{G+1} = \begin{cases} u_i^{G+1} \; if \; f\left(u_i^{G+1}\right) < f\left(X_i^{G}\right) \\ X_i^{G} \qquad\qquad\qquad otherwise \end{cases} \tag{3.13}$$

Where $f(X)$ is the objective function to be minimized, and G is the generation count. Once the selection operation is completed, the algorithm loop is repeated until the stopping criteria is satisfied.

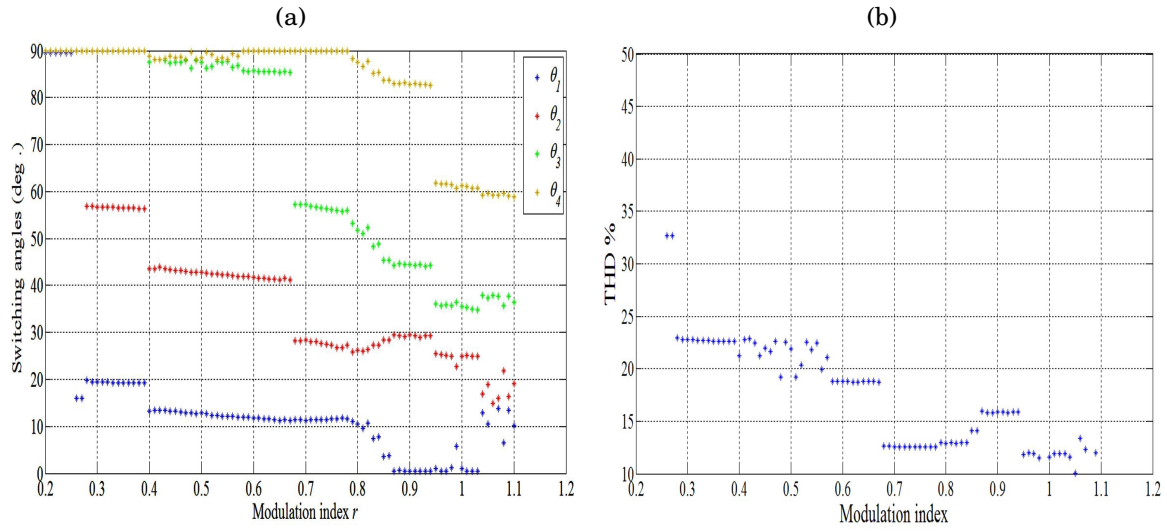

FIGURE 3.7. Switching angles obtained by using DE algorithm versus modulation index (a) THD versus modulation index (b).

Figure 3.7 show the optimal switching angles computed using the DE algorithm versus the modulation index, these results demonstrate the ability of this algorithm of solving the system of non linear system for a wide range of modulation index.

3.1.3 Simulated annealing

The simulated annealing is a stochastic global optimization method that can differentiate between multiple local optima points[92, 93]. The algorithm is inspired from the process

of cooling metal after heating it to get a perfect crystal structure with minimum defects [94].

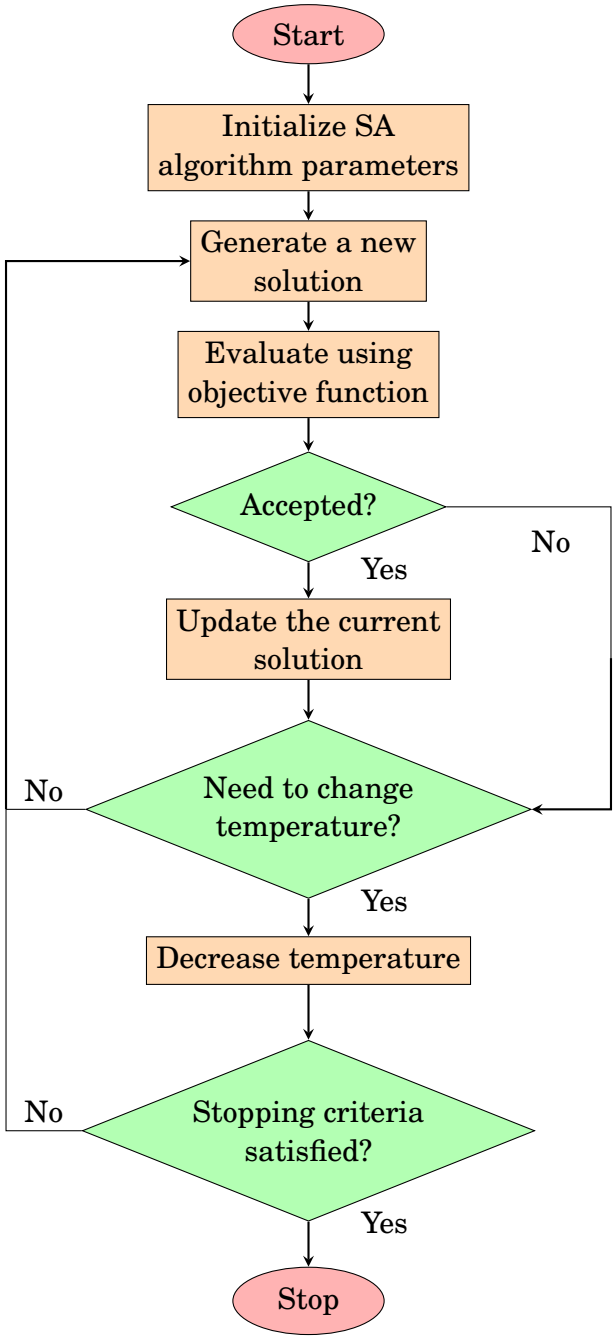

FIGURE 3.8. Simulated annealing algorithm (SA) flowchart.

While many optimization methods get stuck in a local minimum instead of converging

to a global minimum, the simulated annealing solves this problem by performing a random search. Figure3.8 presents a simplified flowchart of the simulated annealing algorithm. The algorithm deals with the minimization of an objective function using a parameter called temperature to evaluate the probability of accepting worst values to escape local minima. The algorithm starts by defining the values of parameters and algorithm operators, and also sets the temperature parameter T to an initial value with initial set of solutions. In this algorithm new random solutions are generated for each iteration, if the newly generated solution improves the objective function f(x) expressed in (2.11) and gave better result than the previous one, then the proposed solution is accepted. Another technique to evaluate the improvement of the system, is to accept the new random solution with a likelihood according to a probability of $e^{(-\Delta f)}$, where Δf is the variation of the objective function, this variation can be expressed by the following equation[95]:

$$\Delta f = f\left(x^k\right) - f\left(x^{k-1}\right) \tag{3.14}$$

Where k is the current iteration.

3.1.4 Harmony search

The harmony search (HS) is a new optimization algorithm inspired by the music improvisation process [96]. It was first introduced in 2001 by Geem in [97] and it was initially used to solve pipe network design problems in 2002 [98]. As a new population-based optimization algorithm the HS has drawn the attention of engineers and scientists all over the world and gained great success in multiple areas of research, especially in process control, electrical power and vision systems [99–102].

It draws inspiration from harmony improvisation, when an artist tries to create harmony; he usually tries different combinations of music pitches on his instrument to obtain better harmony. Composing a perfect harmony is a very similar to the process of finding an optimal result for an optimization problem.

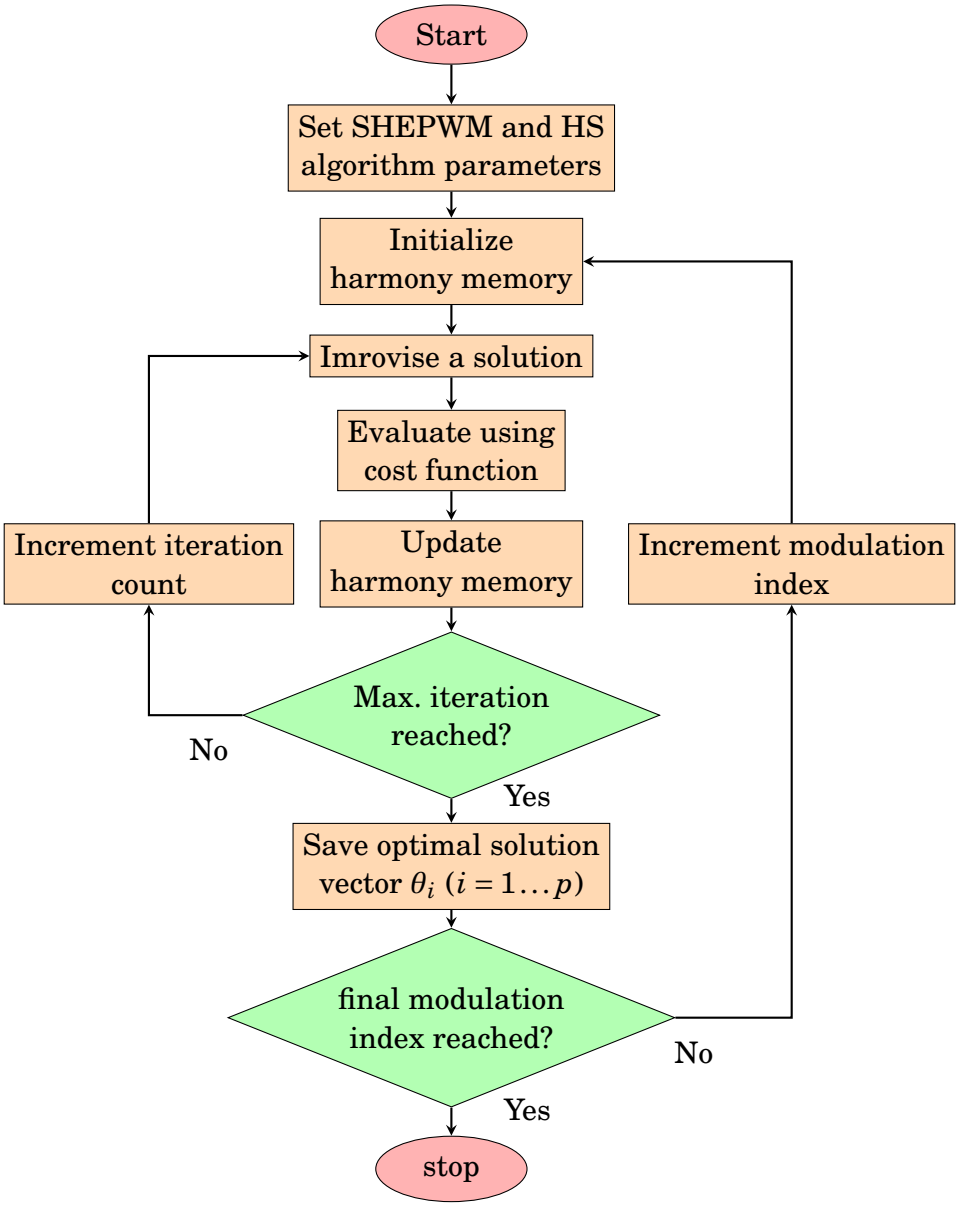

FIGURE 3.9. Harmony search (HS) flowchart for solving SHEPWM problem.

HS depends on two important parameters, harmony memory considering rate (HMCR) and pitch adjusting rate (PAR) [103, 104]. The algorithm is composed of three main steps: harmony memory generation, harmony improvisation, and harmony memory update[105]. In the case of SHEPWM control strategy the HS is used as an optimization tool to perform a random search for the global minima, which means forcing the objective

function (2.11)towards a minimum value. Figure 3.9 demonstrates a flowchart of the HS algorithm used to solve the SHEPWM problem.

The HS algorithm begins by initializing the necessary parameters such as harmony memory size (HMS), HMCR, PAR, upper and lower limits (x_{min} and x_{max}) and the maximum number of improvisations (NI). It should be noted that upper and the lower limits must satisfy Eq. (2.9).The next step is to create the initial harmony memory (HM).

The HM is a memory space in which the possible solutions can be stored. The initial HM matrix consists of many initial solution vectors randomly generated. The initial solutions are generated using the following equation:

$$x = x_{min} + rand(x_{max} - x_{min}) \tag{3.15}$$

rand is a random number with a value ranging from 0 to 1 and x_{min} and x_{max} are minimum and the maximum limit values of the desired solutions. For n dimension and HMS size, harmony memory can be writer as the following expression:

$$HM = \begin{bmatrix} x_1^1 & x_2^1 & \dots & x_n^1 \\ x_1^2 & x_2^2 & \dots & x_n^2 \\ \vdots & \vdots & \vdots & \vdots \\ x_1^{HMS} & x_2^{HMS} & \dots & x_n^{HMS} \end{bmatrix} \tag{3.16}$$

The next step of the algorithm is the solution improvisation. The improvisation of a new set of solutions (harmony vector) $[x_1^i, x_2^i, \dots, x_n^i]$ is based on $HMCR$, PAR, and random selection. The $HMCR$, is the selection rate of a candidate solution stored in the harmony memory (HM), the $HMCR$ can have a value between 0 and 1, it is usually set between 0.7 and 0.95 in order to obtain good results[106]. $(1 - HMCR)$ is the selection rate of a random possible solution. The improvisation process can be written in following expression:

$$x_i \leftarrow \begin{cases} x_i \in \{x_i^1, x_i^2, \dots, x_i^{HMS}\} & \text{with probability } HMCR \\ x_i \in X_i & \text{with probability } (1 - HMCR) \end{cases} \tag{3.17}$$

with $i \in [1,2,\ldots,n]$ and $X_i \in [x_{min},\ldots,x_{max}]$.

If the $HMCR$ value is set to be 0.95 it means that the algorithm will choose the decision variable value from the harmony memory with a probability of 95% or a value form all the possible range (from 0 to $\frac{\pi}{2}$ for the SHEPWM problem) with a probability of $(100-95)\%$. Every element of the obtained solutions is subjected to whether it should be pitch adjusted, which is determined by the PAR, whereas the $1-PAR$ value is the rate of doing nothing. The equation below describes the adjustment operation.

$$\begin{cases} Yes & with\,probability\,PAR \\ No & with\,probability\,(1-PAR) \end{cases} \tag{3.18}$$

If the pitch adjustment decision is $''No''$ the solution x_i will not be modified, if the decision is $''Yes''$ x_i will be replaced using the following equation:

$$x_i = x_i + rand \times b_w \tag{3.19}$$

where $rand$ is a randomly generated number with a value ranging from 0 to 1, and b_w is an arbitrary distance bandwidth.

The next step of the algorithm will be the update of the HM . Once the improvisation is achieved, the stored HM elements must be updated. In this process the HM is updated according to the overall value of the targeted objective function presented in equation (2.11). If the new improvised harmony vector $[x_1^i, x_2^i, \ldots, x_n^i]$ has a better fitness than the worst solution vector in the HM will replace it [107].

The last step of the algorithm is checking the stopping condition, which in this work is the number of improvisations. If the number of improvisations reached the maximum value (NI) , the computation process stops. Otherwise the improvisation and the update processes are repeated.

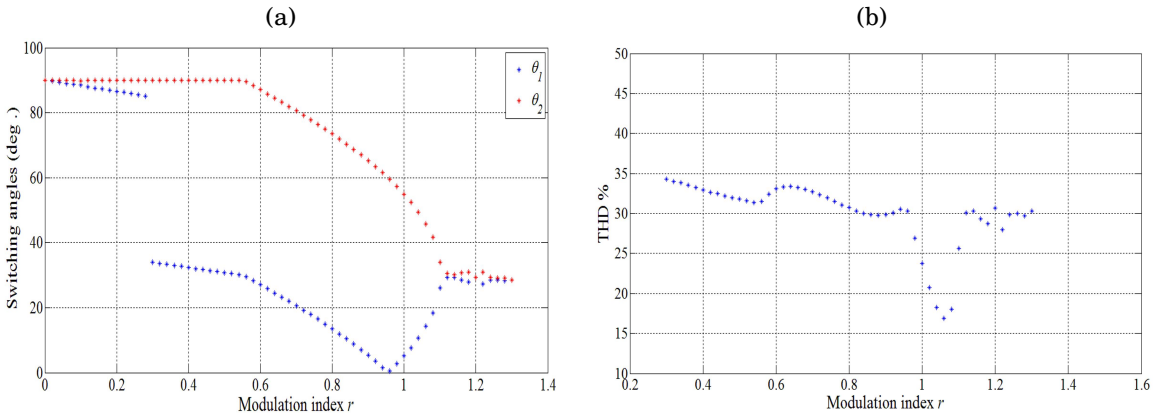

FIGURE 3.10. Five level inverter optimal switching angles obtained by using HS algorithm versus modulation index (a) THD versus modulation index (b).

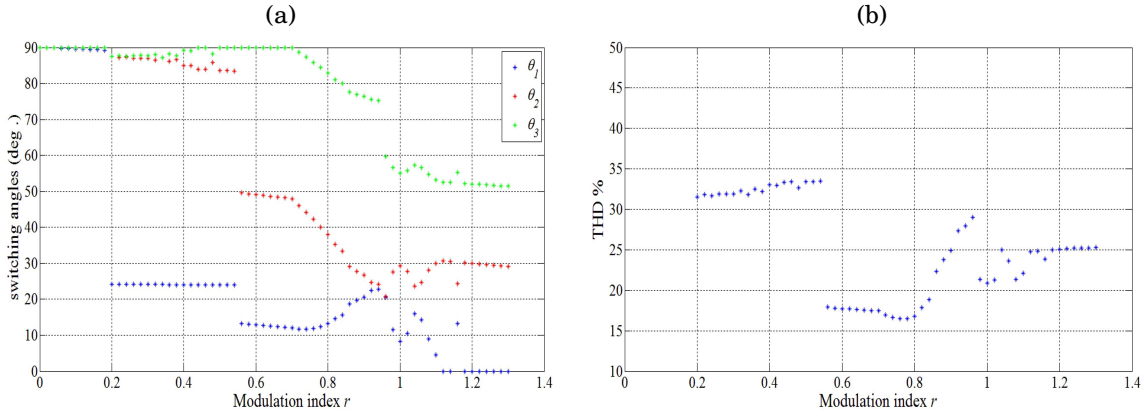

FIGURE 3.11. Seven level inverter optimal switching angles obtained by using HS algorithm versus modulation index (a) THD versus modulation index (b).

Figures 3.10 and 3.11 show the computed optimal switching angles for five and seven level configuration computed using harmony search algorithm versus the modulation, and the resulted total harmonic distortion versus the modulation index, these results demonstrate the ability of the algorithm of solving the optimal switching problem for a wide range of modulation index, it can also be seen from the figures that by increasing the number of voltages, the total harmonic distortion drops in some parts of the modulation

index.

3.2 Application of artificial neural networks

3.2.1 Fundamental theory

3.2.1.1 Biological neurons

The processing of information in a human brain is done by biological processing system composed of different elements, operating in parallel in order to produce function such as learning and thinking. The most basic element of the processing system is called a neuron, and its role is to transmit signals under certain operation conditions. Figure3.12 shows the basic structure of a biological neuron, and it's composed of three main parts:cell body,dendrites and axon. The cell body of the neuron, which includes the neuron's nucleus, is where most of the neural computations happen[108].

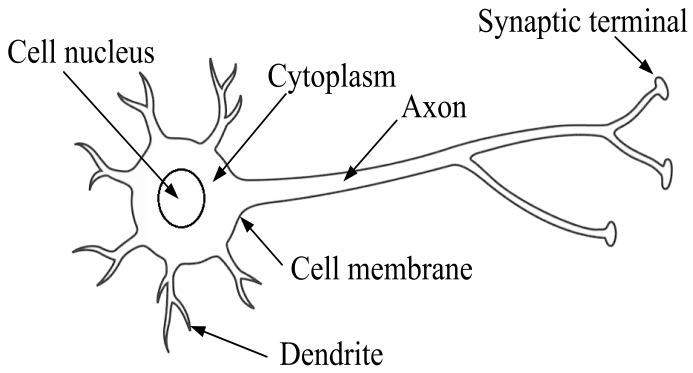

FIGURE 3.12. Structure of a biological neuron.

The role of the synaptic terminals is to transmit the signal from the axon to dendrites of other neurons as demonstrated in figure 3.13 it's worth noting that there are no physical connection between the neurons forming a synaptic junction, so the neurotransmitter elements released from the synaptic terminals are in charge of weighting the transmission from the synaptic space to the dendrites of the next neuron.

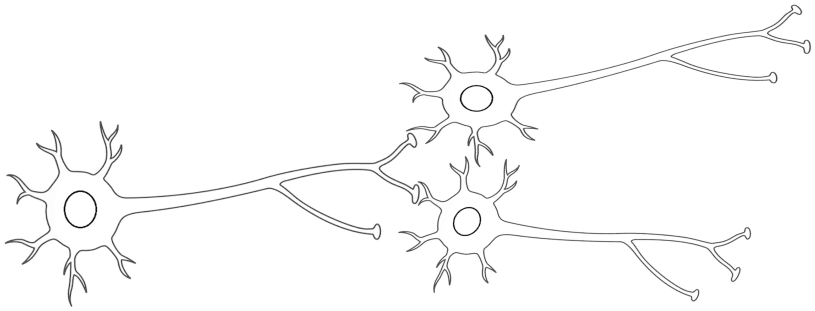

FIGURE 3.13. Structure of a biological neuron.

3.2.1.2 Artificial neurons

Artificial neural networks (ANNs) are mathematical functions modeled after biological neural networks. the processing elements of an ANN are called artificial neurons.The ANNs imitate the mechanism of the brain. As the biological network (brain) is composed of connections of multiple biological neurons, an artificial neural network is built using elements that correspond to biological neurons called nodes.

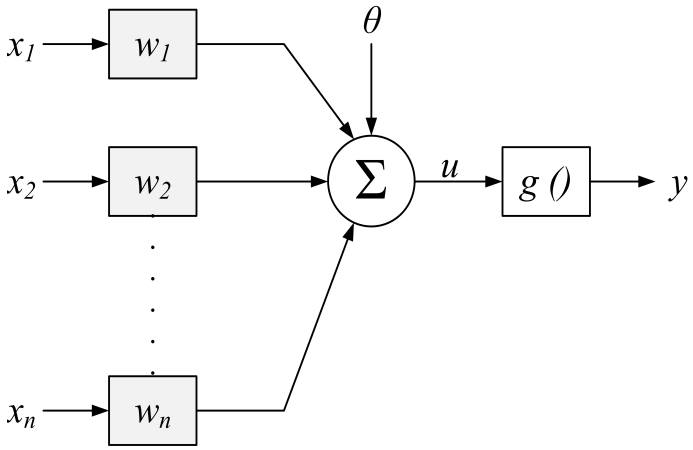

FIGURE 3.14. Structure of an artificial neuron.

$[x_1, x_2, \ldots, x_n]$ are the input signals or samples coming from the external environment, w_1, w_2 and w_n are the weights of each corresponding input, and θ is is the bias.
The input signals coming from the external environment are multiplied by the weights

before they reach the summing node ($\sum$). The weighted sum u is called "activation potential" and it can be expressed by the following equation:

$$u = \sum_{i=1}^{n} x_i.w_i + \theta \tag{3.20}$$

The output signal (y) expressed in equation (3.21) is the final result generated by the network, this signal can also be used as an input to another network.

$$y = g(u) \tag{3.21}$$

g is known as "activation function" and its role is to limit the value of the generated output within a reasonable range.

3.2.2 Main artificial neural network topologies

3.2.2.1 Single layer feed-forward topology

The single layer neural network topology is composed as its name suggests of one neural layer which is also the output layer. Figure(3.15) presents the generalized single layer topology, composed of n inputs and m outputs. The number of neurons that can be used in this topology correspond to the number of outputs. this architecture is often used in classification, system identification and pattern recognition problems[109–111].

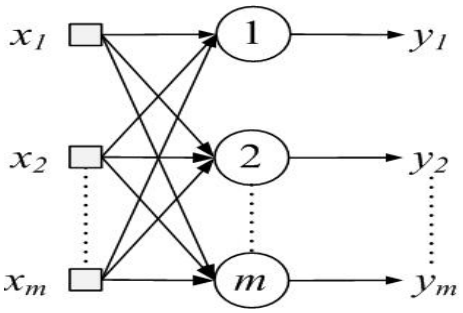

FIGURE 3.15. Single layer feed-forward topology.

3.2.2.2 Multiple layer feed-forward topology

Unlike the previous architecture, the multiple layer topology has multiple hidden layers and an output layer as figure (3.16) shows. This configuration is usually used for pattern

recognition classification, system identification, process control, optimization and robotics [112–120] .

Figure (3.16) shows an example of a multiple layer neural network topology composed of a single input layer with n inputs, two hidden layers composed of n_1 and n_2 neurons respectively and a single output neural layer composed of m neurons.

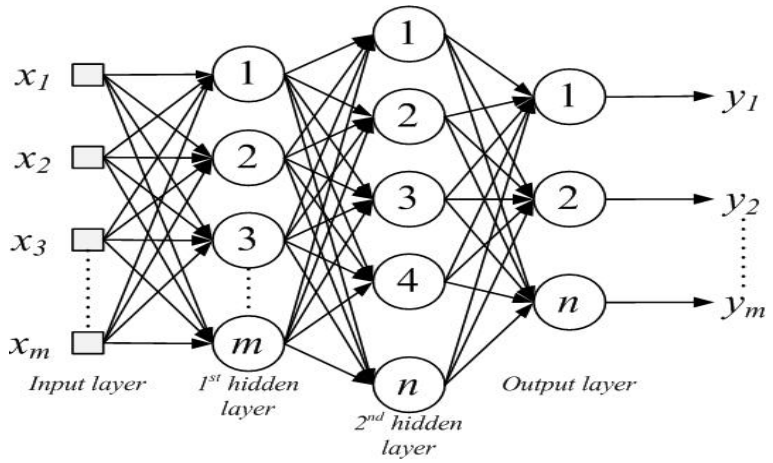

FIGURE 3.16. Multiple layer feed-forward topology.

it can be noticed from figure(3.16) that the number of neurons used to construct the hidden layers can be different from the number of signals composing the input or output layer, in fact the hidden layer size depends on the complexity of the problem being mapped by the ANN.

3.2.3 Training Process

One of the most important features of artificial neural networks is their ability to learn. 'Learning' or 'training' process, forms the the interconnections between the different neurons in the network. This process can be done by providing input and output data (also known as targets) collected from the system or the problem to be mapped. The network then is given a learning algorithm to follow and to compute the new weights that will lead the generated output value closer to the given target.

Artificial neural networks can be a subject to either unsupervised or supervised learning.

The unsupervised learning method does not require the knowledge of the desired output values, this method is usually used for density estimation (statistics) [121] and communication systems [122].
Different from unsupervised learning supervised leaning method require as mentioned previously the knowledge of desired output values for a given set of inputs. These input/output data sets will act as teacher for the artificial network. The weights $\{w_1, w_2, \ldots, w_n\}$ and thresholds of the neural network are constantly tuned during the training process, executed by a learning algorithm that supervises the difference between the generated values and given targets with respect to the desired input signals.

3.2.4 Real-time selective harmonic elimination using artificial neural networks

ANNs are a very efficient tool inspired by the behavior of biological neurons; these neurons can be trained to execute a particular task by adjusting the width of the connections (also called weights) between nodes. As mentioned before, the purpose of using ANNs is to perform online SHEPWM control of the multilevel inverter. Figure 3.18 demonstrates the ANN structure proposed in this work. The proposed ANN structure consists of three layers: input layer, hidden layer, and output layer. The input layer is formed by a single node and takes the desired modulation index r as input. The output layer is formed by ten nodes that correspond to the switching angles.The neural networks are trained so that the input (modulation index) leads to a desired output (switching angles). The training process (flowchart presented in figure 3.17) requires the knowledge of a vast set of switching angles and their corresponding modulation indices.

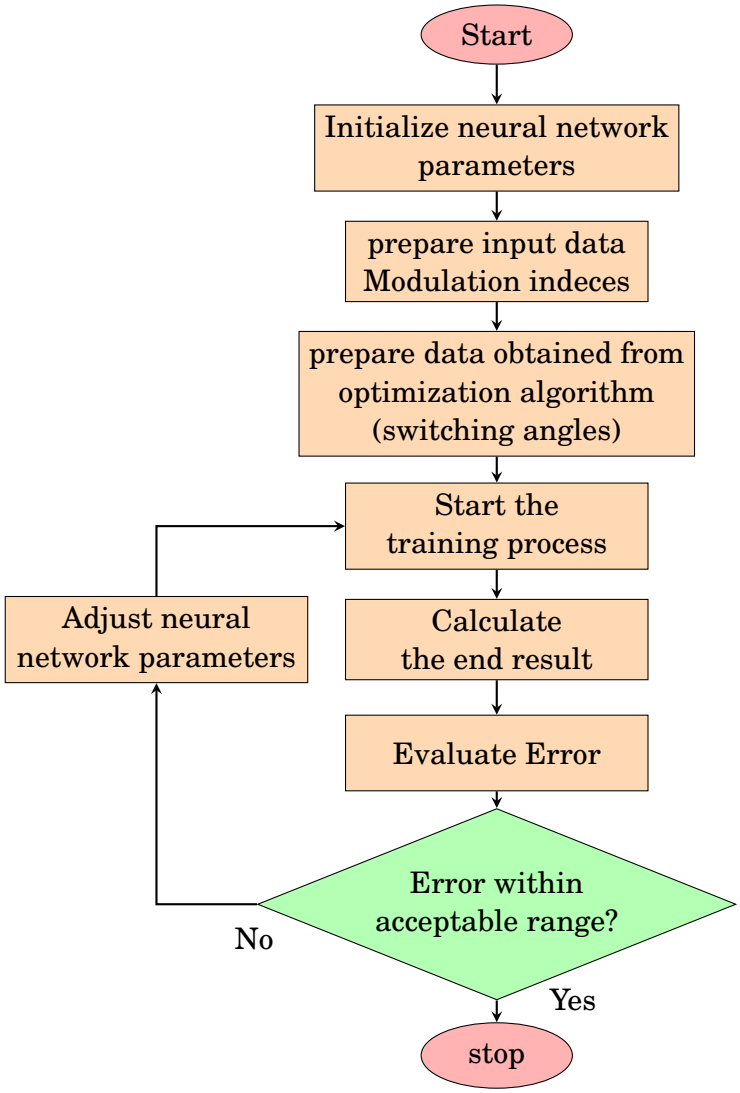

FIGURE 3.17. Artificial neural network training process for the SHEPWM problem.

In this process, the weights (the connection between the nodes) are adjusted, based on a comparison of the output generated by the neural networks for each modulation index and the switching angles obtained by the optimization algorithm, until the network output matches the data set obtained by the optimization algorithm.

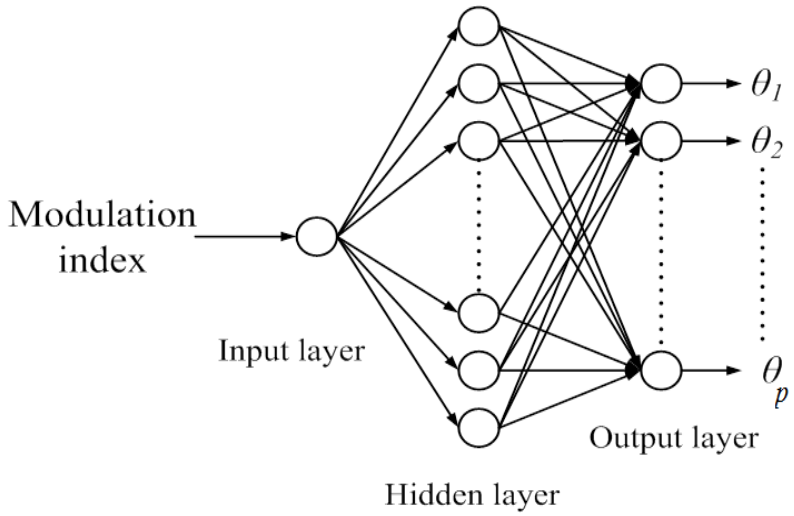

FIGURE 3.18. Block diagram of the ANN based SHEPWM mechanism

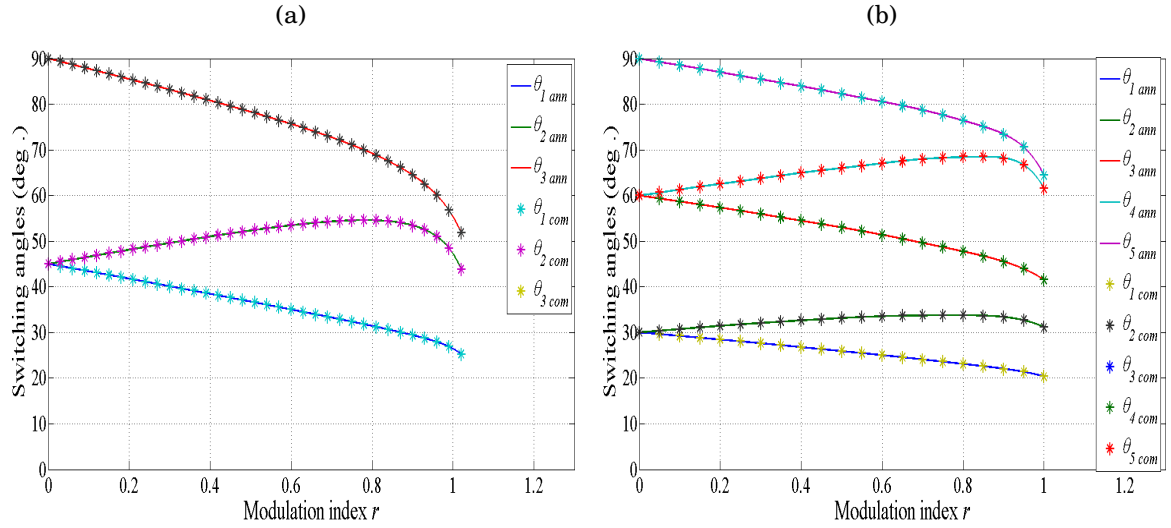

FIGURE 3.19. Comparison between switching angles generated by optimization algorithm and artificial neural networks (for three switching angles left, five switching angles right).

Figure 3.19 shows switching angles generated by optimization algorithm and artificial neural networks for a system with three and five switching angles, it can be seen from the figure that the artificial neural networks, were not only able to generate the same

switching angles but also create intermediate results which allows us to use those networks to control inverters in real-time.

3.3 Conclusion

This chapter focused on the different methods used to solve the optimal switching problem (SHEPWM). As mentioned before, optimization algorithms offer a lot of advantages compared to analytical such as the ability to converge towards a solution or multiple solutions without the need for initial guess and the ability to escape local minima. The chapter demonstrates also a real-time selective harmonic elimination based on artificial neural networks, using this method can be useful in the case of studying these systems, this approach allows us to generate solutions instantly without the need for computation methods. This method will be applied on the proposed multilevel topology in the next chapter.

CHAPTER 4

SIMULATION AND EXPERIMENTAL RESULTS

Simulation and computer calculations have been extensively used in this chapter to develop the proposed control methods. Multiple prototypes of multilevel inverters have been built to validate the calculations obtained by optimization methods. The developed prototypes and control methods have been the subject of extensive tests. The chapter starts by showing simulation and experimental results of applying the SHEPWM strategy on a five, seven and nine multilevel inverter in order to show the impact of increasing the number of voltage levels on waveform quality. Then we discuss the possibility of using passive filters and their influence on the harmonic performance of the converters. The chapter ends by presenting the proposed multilevel inverter topology is a hybrid asymmetric multilevel topology with reduced device count converter. The topology generates up to 21 voltage levels, combining this feature with the selective harmonic elimination modulation method will lead to an excellent harmonic performance, which makes the use of passive filters unnecessary.

4.1 Application of selective harmonic elimination on multilevel inverters

In this section, tests were carried out on multiple configurations of the cascaded H-bridge topology demonstrated in figure 4.1, the number of voltage levels is increased each time in order to see its influence on the waveform quality. A small scale prototype of the cascaded converter was built in order to validate the obtained simulation results.

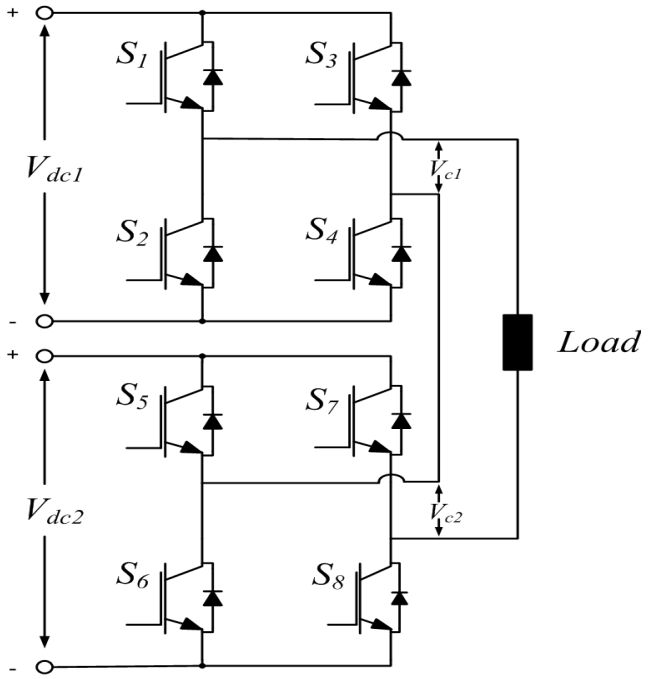

FIGURE 4.1. Circuit of the CHB converter used in the experiment

4.1.1 Five level inverter

In this case the input voltages of the converter are equal (V_{dc1}=V_{dc2}), which allows us to obtain a five level voltage waveform. Table 4.1 shows the switching states for each voltage level.

Table 4.1: Output voltage levels ($p.u.$) with corresponding conducting switches for the a 5-level asymmetric cascaded inverter.

Voltage ($p.u.$)	**Switches in (ON) state**
2	S_2, S_4, S_6, S_7
1	S_2, S_3, S_6, S_8
0	S_2, S_4, S_6, S_8
-1	S_1, S_4, S_6, S_8
-2	S_2, S_4, S_5, S_8

The system of non linear equations that describes the uniform five level waveform can be written as follows:

$$\begin{cases} H_1 = \cos(\theta_1) + \cos(\theta_2) = M \\ H_2 = \cos(3\theta_1) + \cos(3\theta_2) = 0 \end{cases} \tag{4.1}$$

Where H_1 is the fundamental component and H_2 is the 3^{rd} harmonic. In this case the system allows us to control the fundamental and eliminate a single harmonic since there are only two switching angles. The third harmonic was set to be eliminated because it has the highest amplitude in the spectrum. The system was previously solved for multiple values of M. Figures 4.2 and 4.3 show the generated voltage waveform and the corresponding FFT analysis (simulation and experimental) for r=0.75.

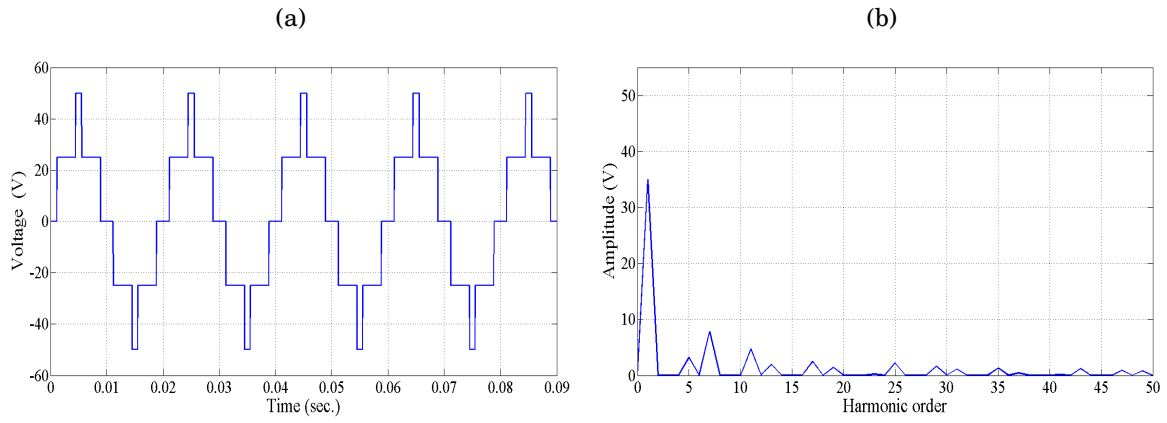

FIGURE 4.2. Output voltage waveform and the corresponding FFT of 5-level H-bridge inverter

(a) (b)

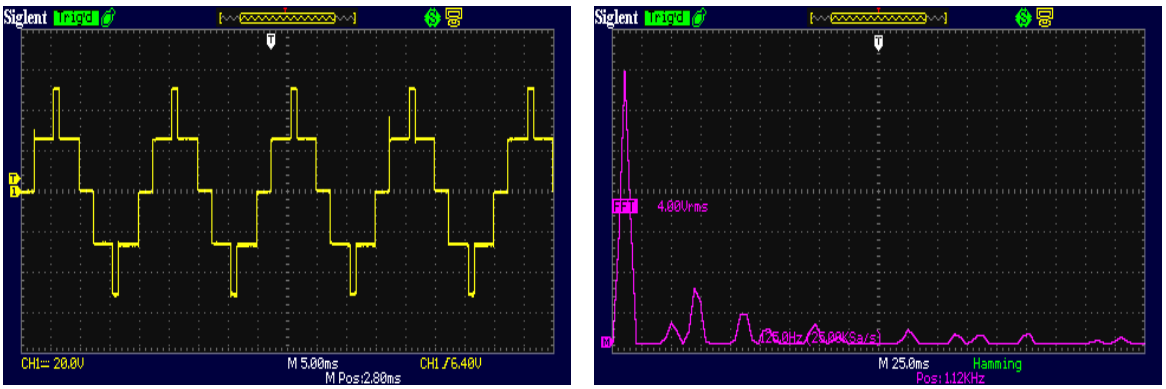

FIGURE 4.3. Output voltage waveform and the corresponding FFT of 5-level H-bridge inverter

It can be seen from the obtained simulation and experimental results that the targeted harmonic has been successfully eliminated.

4.1.2 Seven level inverter

In a seven level asymmetric configuration the voltage of the second power source (V_{dc2}) must be twice the voltage of (V_{dc1}).The switching states of the semiconductor devices for are presented in table 4.2 .

Table 4.2: Output voltage levels ($p.u.$) with corresponding conducting switches for the a 7-level asymmetric cascaded inverter.

Voltage ($p.u.$)	**Switches in (ON) state**
3	S_2, S_3, S_6, S_7
2	S_2, S_4, S_6, S_7
1	S_2, S_3, S_6, S_8
0	S_2, S_4, S_6, S_8
-1	S_1, S_4, S_6, S_8
-2	S_2, S_4, S_5, S_8
-3	S_1, S_4, S_5, S_8

$$\begin{cases} H_1 = \cos(\theta_1) + \cos(\theta_2) + \cos(\theta_{10}) - m = 0 \\ H_2 = \cos(3\theta_1) + \cos(3\theta_2) + \cos(3\theta_{10}) = 0 \\ H_3 = \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_{10}) = 0 \end{cases} \tag{4.2}$$

Figure 4.4 presents the obtained simulation (top) and experimental results (bottom), it can be clearly seen that the results are in perfect agreement. All the targeted harmonics (3^{rd} and 5^{th}) were eliminated

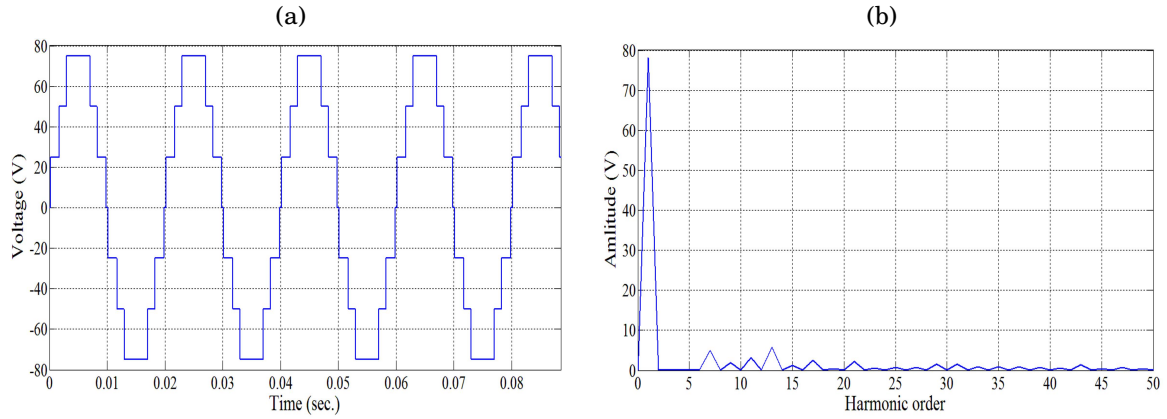

FIGURE 4.4. Output voltage waveform and the corresponding FFT of 7-level H-bridge inverter

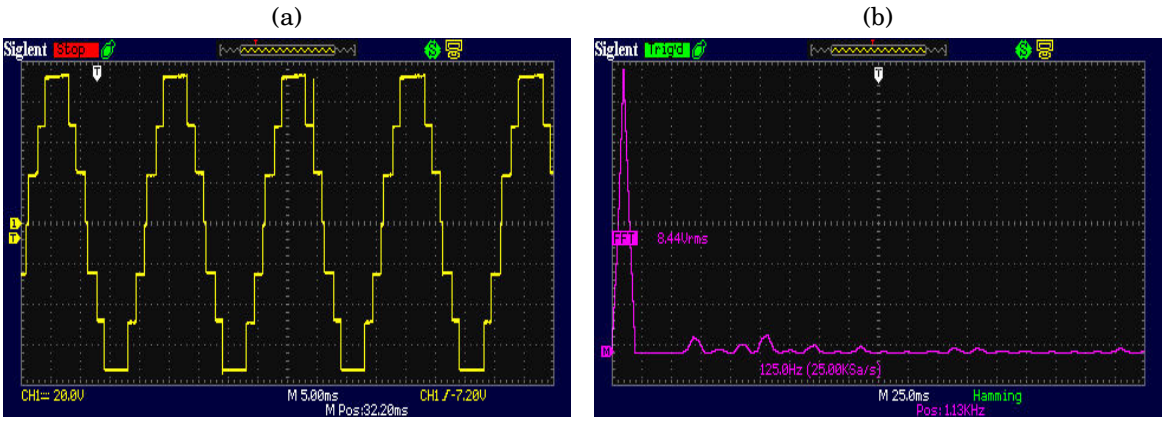

FIGURE 4.5. Output voltage waveform and the corresponding FFT of 7-level H-bridge inverter2

Figures 4.6(a), 4.6(c), 4.6(b) and 4.6(d) show respectively simulation and experimental results of the generated voltage patterns generated by the upper bridge and experimental results of the generated voltage patterns generated by the lower bridge for the seven level asymmetric configuration. Simulation results fit perfectly the obtained experimental results. Both bridges generate same number of voltage levels with different patterns in order to generate the seven level voltage waveforms.

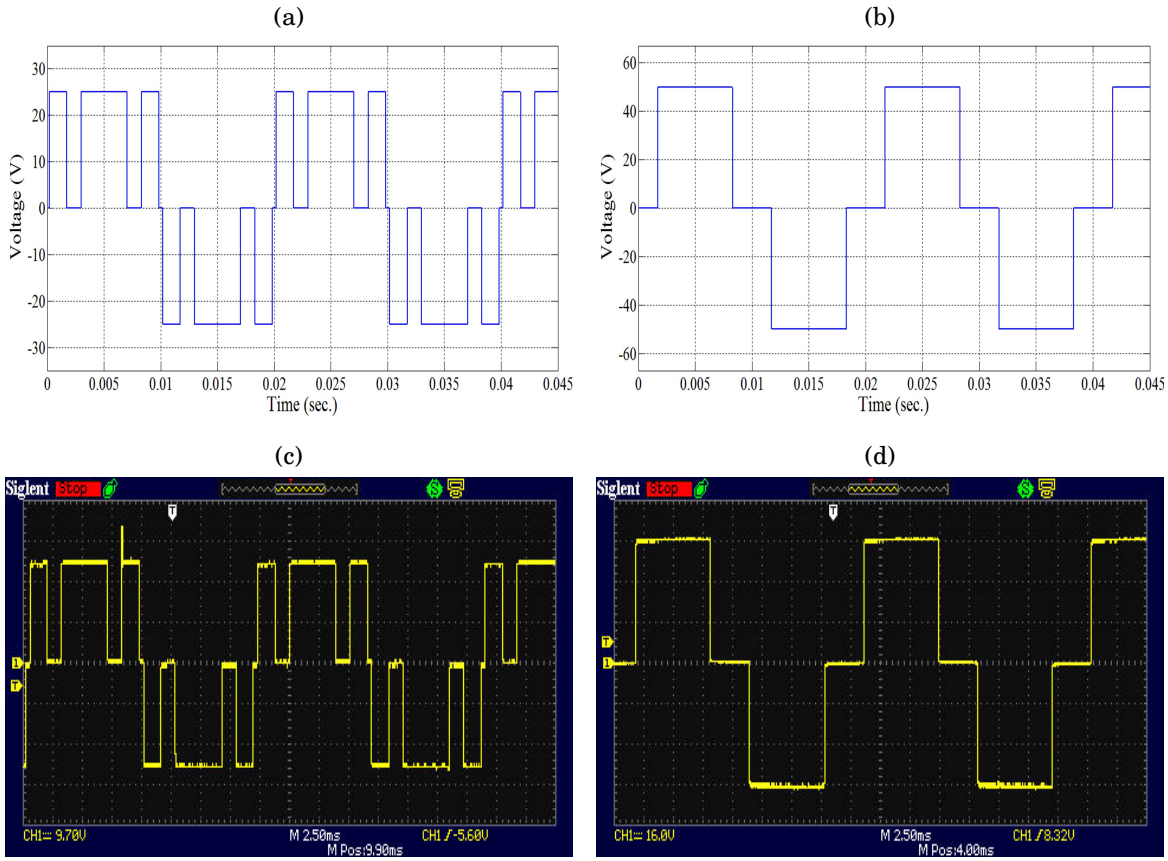

FIGURE 4.6. Voltage waveforms generated by the upper and lower cells of the 7-level H-bridge inverter

4.1.3 Nine level inverter

In the case of the nine level asymmetric configuration the voltage across the lower H-bridge must be three times the value of the upper one ($V_{dc2} = 3 \times V_{dc1}$) to obtain the desired voltage waveform.

Table 4.3: Output voltage levels ($p.u.$) with corresponding conducting switches for the a 9-level asymmetric cascaded inverter.

Voltage ($p.u.$)	**Switches in (ON) state**	**Voltage ($p.u.$)**	**Switches in (ON) state**
4	S_1,S_4,S_5,S_8	-1	S_2,S_3,S_6,S_8
3	S_2,S_4,S_5,S_8	-2	S_1,S_4,S_6,S_7
2	S_2,S_3,S_5,S_8	-3	S_2,S_4,S_6,S_7
1	S_1,S_4,S_6,S_8	-4	S_2,S_3,S_6,S_7
0	S_2,S_4,S_6,S_8		

Simulation and experimental results of the generated waveforms and FFT analysis presented in figure 4.7 show that all undesired harmonics are successfully eliminated.

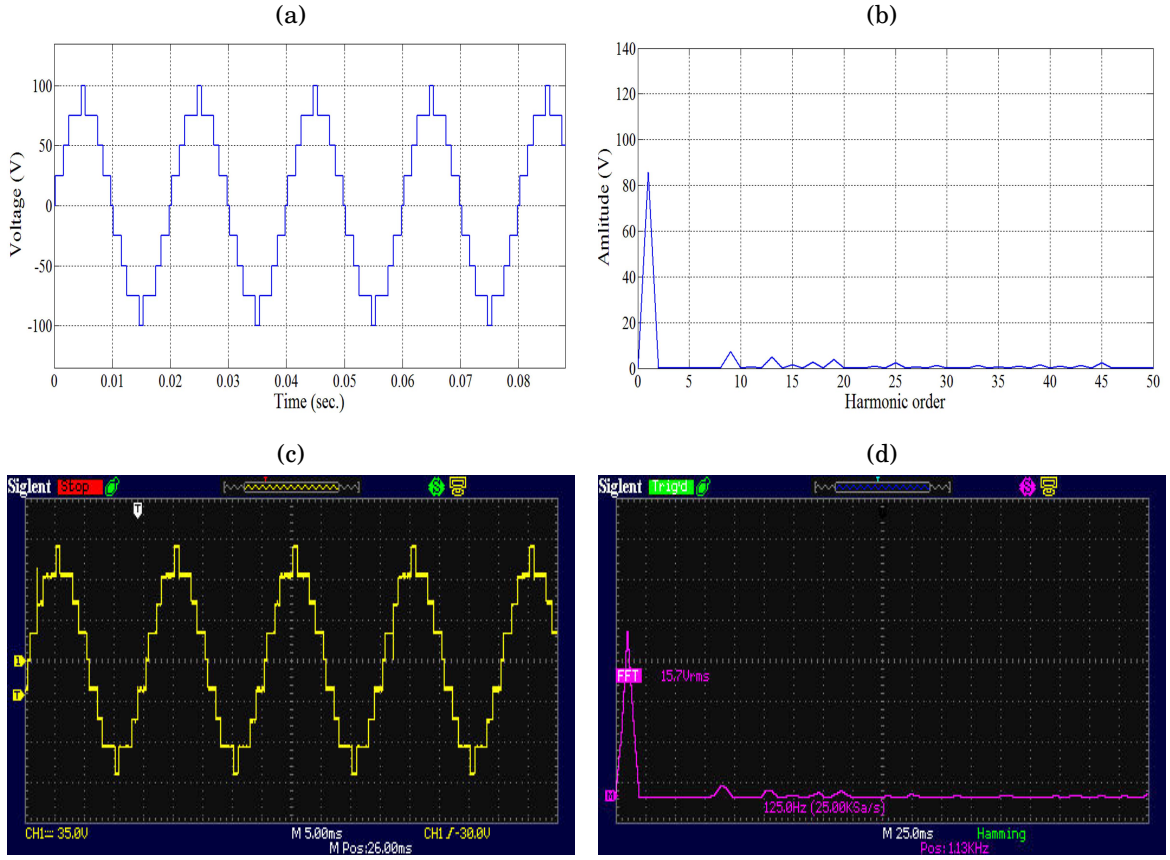

FIGURE 4.7. Output voltage waveform and the corresponding FFT of 9-level H-bridge inverter

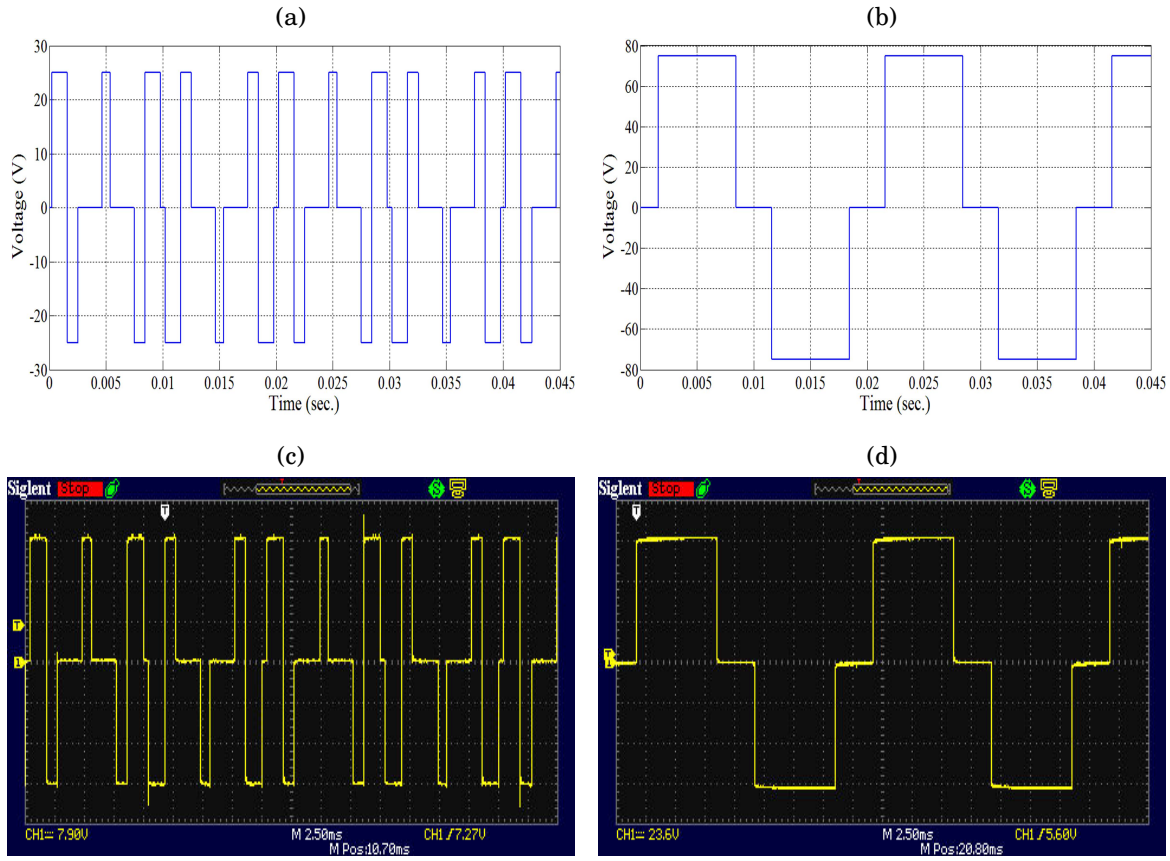

FIGURE 4.8. Voltage waveforms generated by the upper and lower cells of the 9-level H-bridge inverter

Figures 4.8(a),4.8(b),4.8(c)and 4.8(d) present respectively the simulated voltage waveforms generated by the upper and the lower cell and experimental results of the voltage waveforms generated by the same modules, It can be seen that the lower module functions the same way as the seven level configuration, generating a simple three level voltage waveform. Similar to the seven level configuration, the upper module generates a three level waveform but in a different pattern, adding and subtracting the voltage values is what allows us to generate the nine level waveform.

4.1.4 Selective harmonic elimination for three phase inverter

In this experiment the selective harmonic elimination strategy was test was tested on a three phase seven level asymmetrical inverter. and since the triplen harmonics (the odd multiples of the third harmonic) are naturally eliminated in a three phase system.
The system tested in this experiment is a three phase seven level asymmetric inverter. Each phase consists of two H-bridge module connected in series with unequal DC voltage sources. Figure 4.9 shows the block diagram of the experiment .

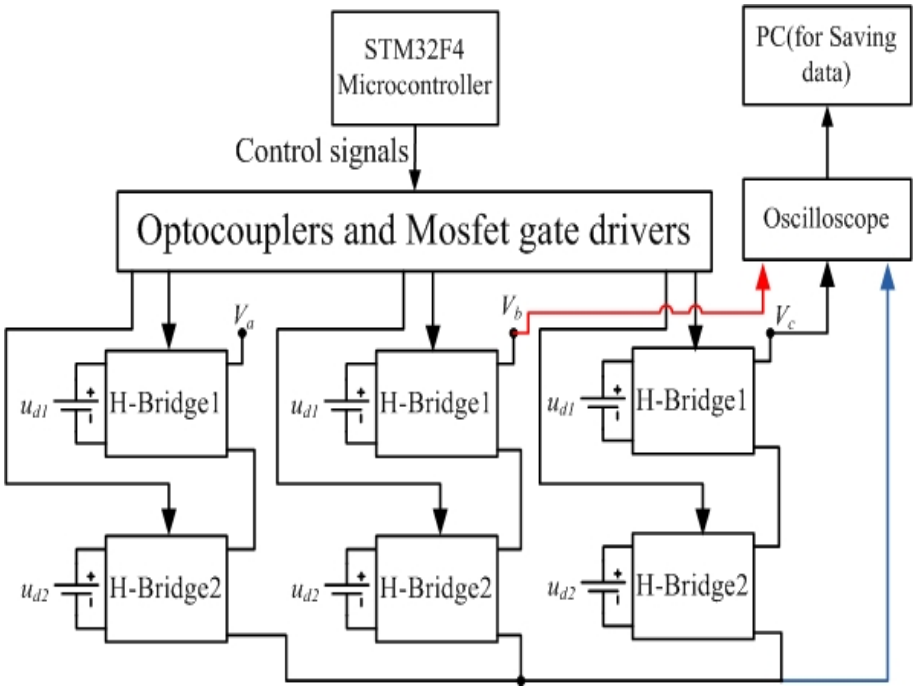

FIGURE 4.9. Block diagram of the experiment

As mentioned earlier in a three phase system, the triplen harmonics are naturally eliminated, therefore there is no need to eliminate them using the SHEPWM. So, the set of non linear equations representing the system can be written as follows:

$$\begin{cases} H_1 = \cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) = M \\ H_2 = \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) = 0 \\ H_3 = \cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) = 0 \end{cases} \tag{4.3}$$

Where H_1,H_2 and H_3 present respectively the fundamental component, the 5^{th} and the 7^{th} harmonic.The system was solved for multiple modulation indices using the harmony search method.

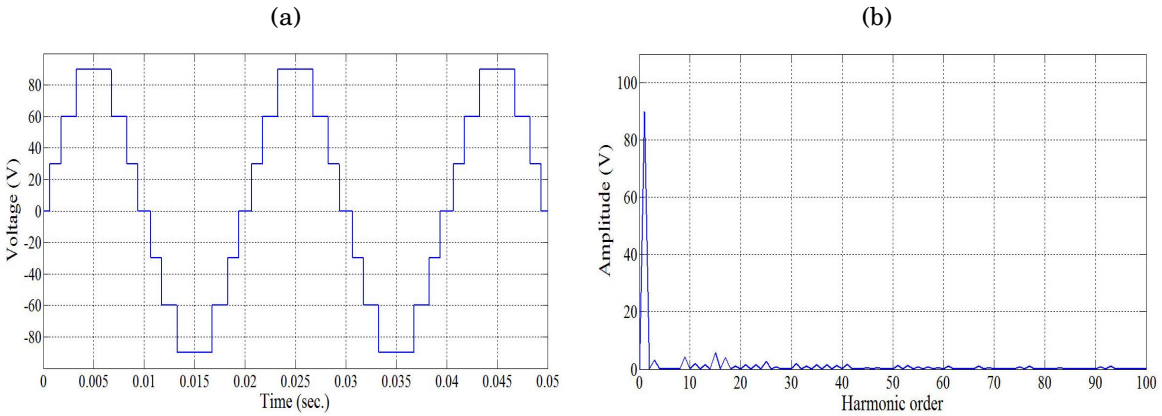

FIGURE 4.10. Simulated output voltage (phase to neutral) waveform and the corresponding FFT of three phase 7-level H-bridge inverter with m=1

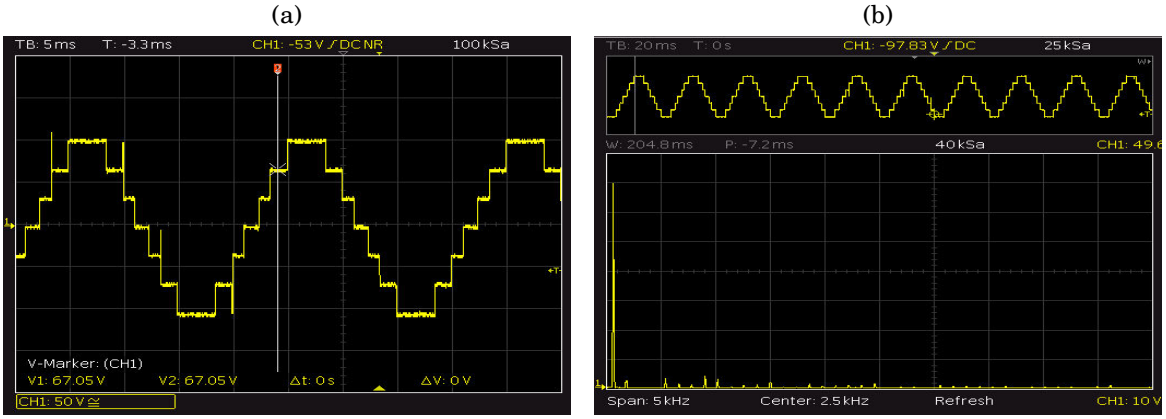

FIGURE 4.11. Output voltage (phase to neutral) waveform and the corresponding FFT of three phase 7-level H-bridge inverter with m=1

Figures 4.10 and 4.11 show simulated and experimental results of the generated phase to neutral voltage waveforms and the corresponding FFT analysis for a modulation index of r=1. The simulation and the experiments results are in good agreement according

to the figures. The FFT analysis shows that the targeted harmonics (5^{th} and 7^{th}) are successfully eliminated. Figures 4.12 and 4.13 show simulated and experimental results of phase to phase voltage waveform and the corresponding FFT analysis for the same modulation index, it can be seen from the FFT analysis that triplen and the targeted harmonics are completely eliminated.

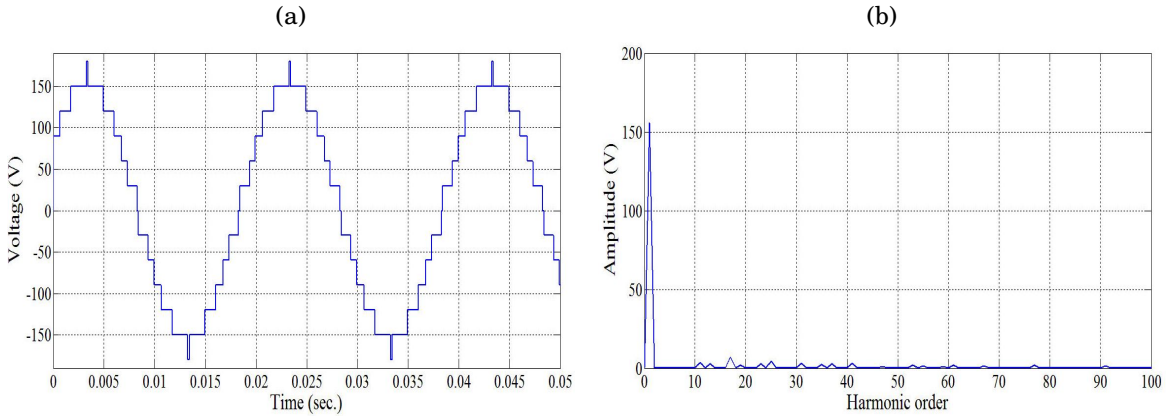

FIGURE 4.12. Simulated output voltage (phase to phase) waveform and the corresponding FFT of three phase 7-level H-bridge inverter with m=1

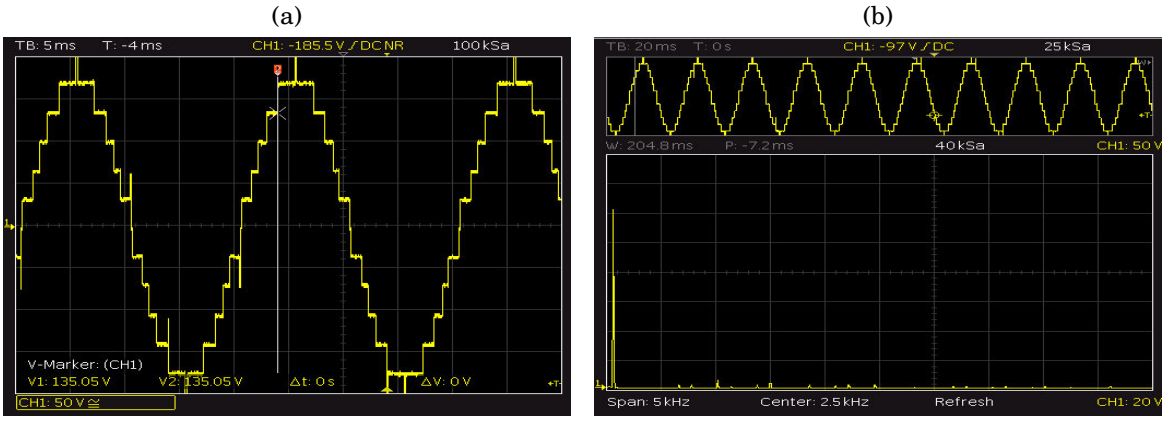

FIGURE 4.13. Output voltage (phase to phase) waveform and the corresponding FFT of three phase 7-level H-bridge inverter with m=1

In order to demonstrate the ability to control the fundamental component using the SHEPWM for a three phase system, the value of modulation index is reduced, the

resulting switching angles were applied to the mathematical model of the system and the prototype. Figure 4.14,4.15,4.16 and 4.17 show simulated and experimental results of the generated phase to neutral and phase to phase voltage waveforms and the corresponding FFT analysis for a modulation index of r=0.5. The experimental results match perfectly the obtained simulation results.

(a) (b)

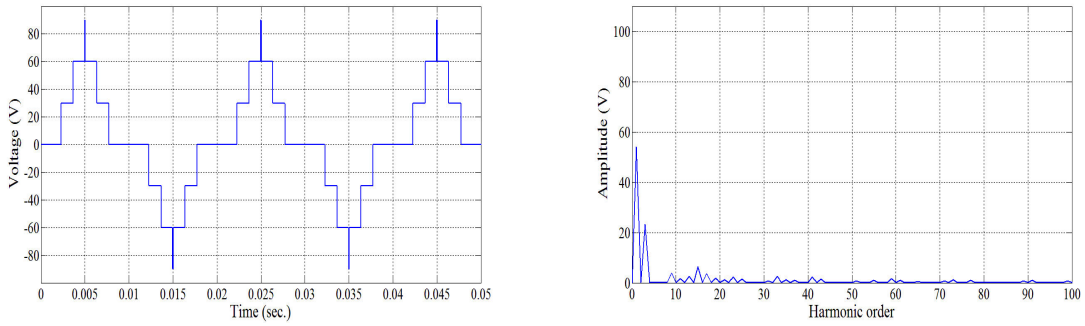

FIGURE 4.14. Simulated output voltage (phase to neutral) waveform and the corresponding FFT of three phase 7-level H-bridge inverter with m=0.5

(a) (b)

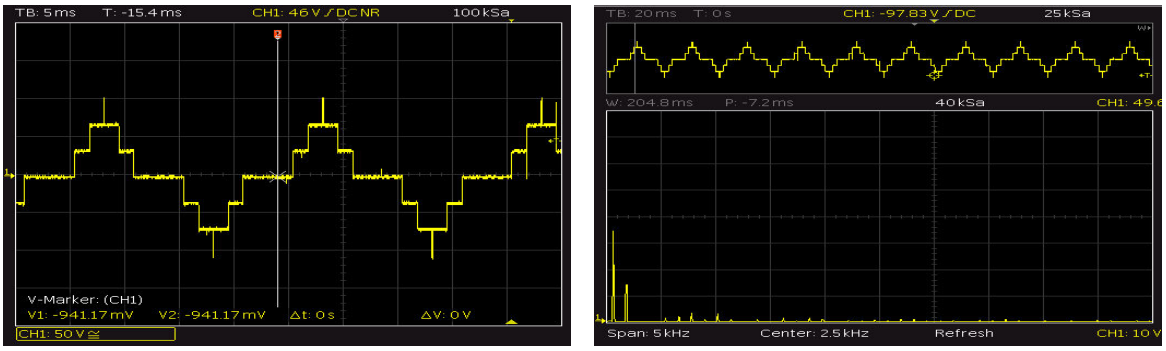

FIGURE 4.15. Output voltage (phase to neutral) waveform and the corresponding FFT of three phase 7-level H-bridge inverter with m=0.5

It can be clearly seen from the FFT analysis results that the value of fundamental component has been significantly reduced compared to the fundamental value for r=1. It can also be noticed that the targeted harmonics were successfully eliminated as expected.

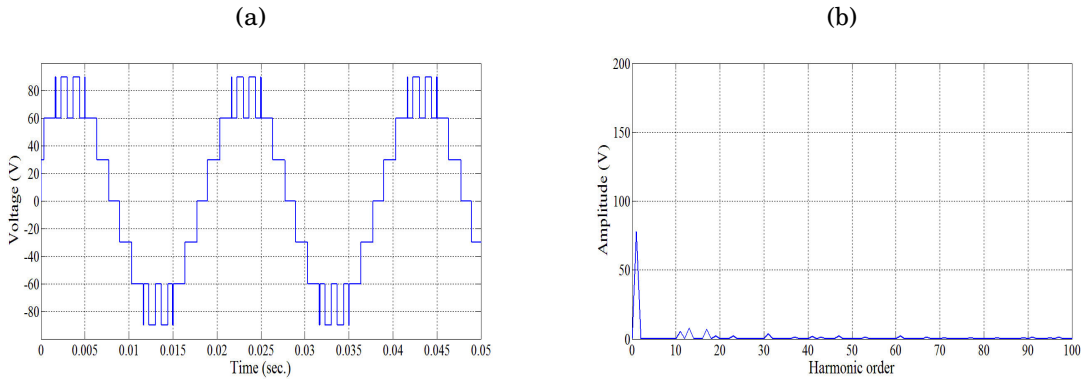

FIGURE 4.16. Simulated output voltage (phase to phase) waveform and the corresponding FFT of three phase 7-level H-bridge inverter with m=1

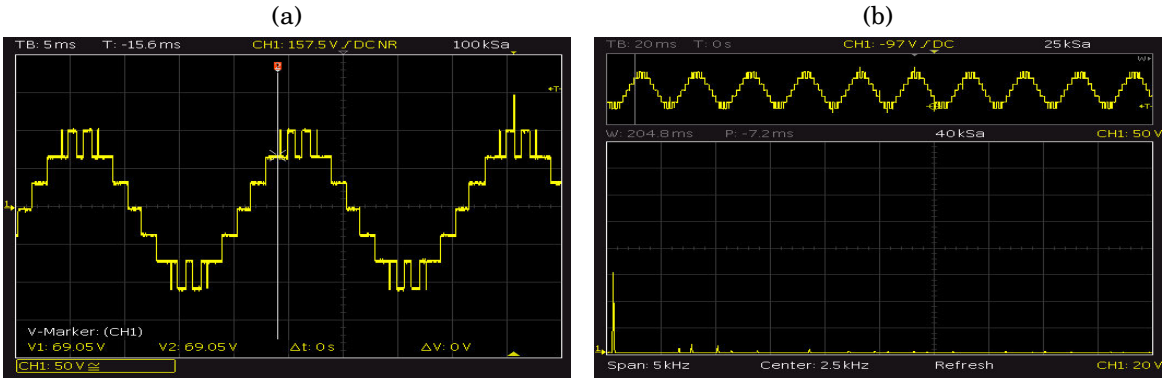

FIGURE 4.17. Output voltage (phase to phase) waveform and the corresponding FFT of three phase 7-level H-bridge inverter with m=0.5

4.2 Application of SHEPWM and passive filters

In this section we study the effect of adding LC filters on the waveform quality. The aim of adding LC filters is to smooth the generated waveform and to eliminate high order harmonics while the selective harmonic elimination strategy eliminates the low order harmonics. The number of voltage levels is increased in order to observe any significant change in the waveform quality. A laboratory prototype is built to validate simulation results.

4.2.1 proposed topology

Figure 4.18 illustrates the structure of the proposed single-phase inverter, it consists of two H-bridge modules connected in series. V_{dc1} and V_{dc2} are the isolated DC voltage sources for the H-bridge modules. An LC filter is added to each of the modules as the figure demonstrates.In this study the inverter is operated in two configurations 5-level and 7-level in order to observe the impact of adding more voltage levels on the quality of the generated AC voltage waveform, and also adding and removing the filters to observe their effect on the output voltage.

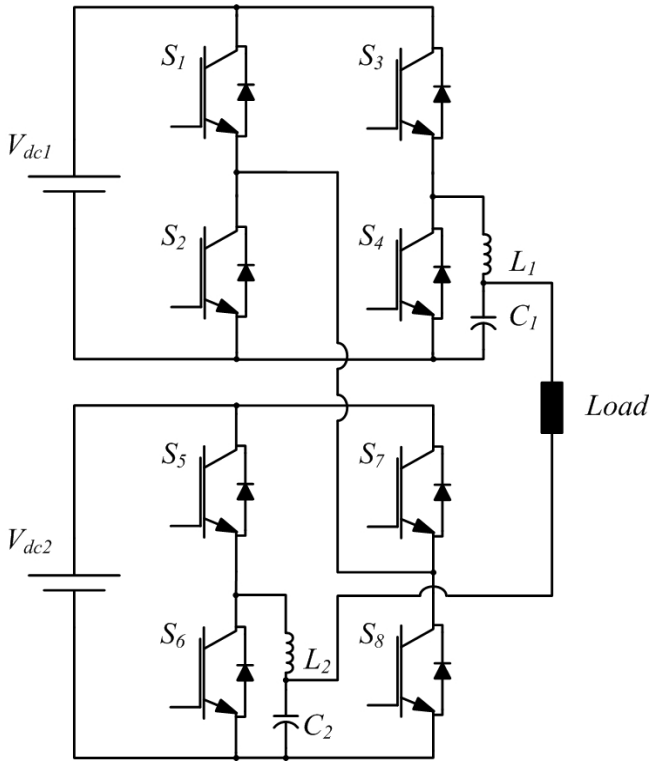

FIGURE 4.18. Proposed multilevel inverter with LC filter

A laboratory prototype of a proposed single-phase CHB multilevel inverter was built using IRF840 (500V, 8A) MOSFETs as the switching devices, and IR2112 as MOSFET gate drivers, 4N25 optoisolators for protection, and two laboratory variable power supplies. Atmel SAM3X8E microcontroller was used to generate control signals. SDS1000 siglent digital storage oscilloscope was used to capture voltage signals. Fast

Fourier Transform (FFT) and THD calculations were performed by computer linked to the SDS1000 digital oscilloscope via USB connection. Fig. 8 shows the experimental setup used in this study.

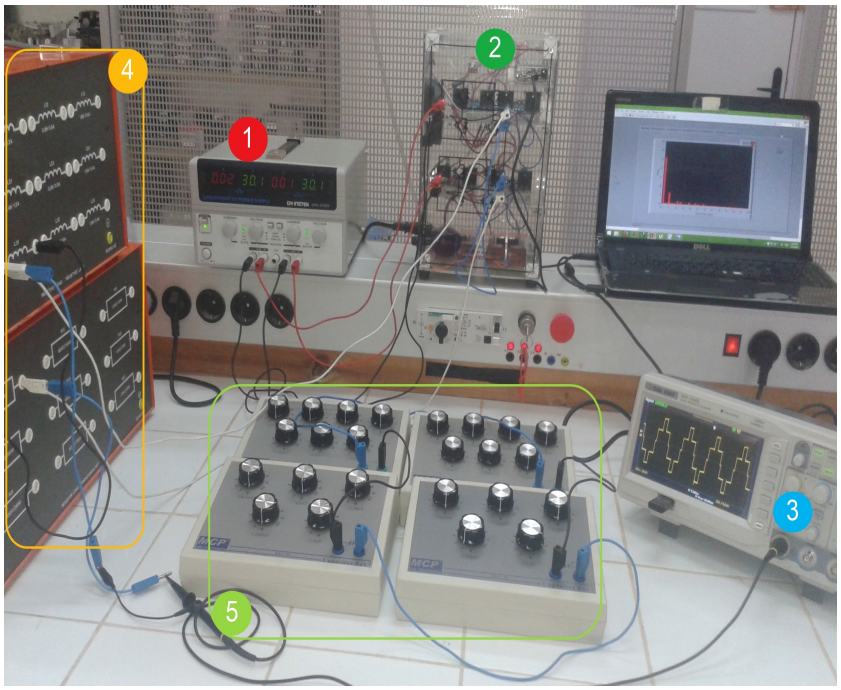

FIGURE 4.19. Experimental setup of the Proposed multilevel inverter with LC filter

❶ DC power supply ❷ Multilevel inverter ❸ Oscilloscope ❹ Load ❺ LC filters

4.2.2 Five level configuration

The 5-level configuration can be achieved by using equal DC sources (V_{dc1} =V_{dc2}) The voltage levels for this configuration are generated using table 4.1.

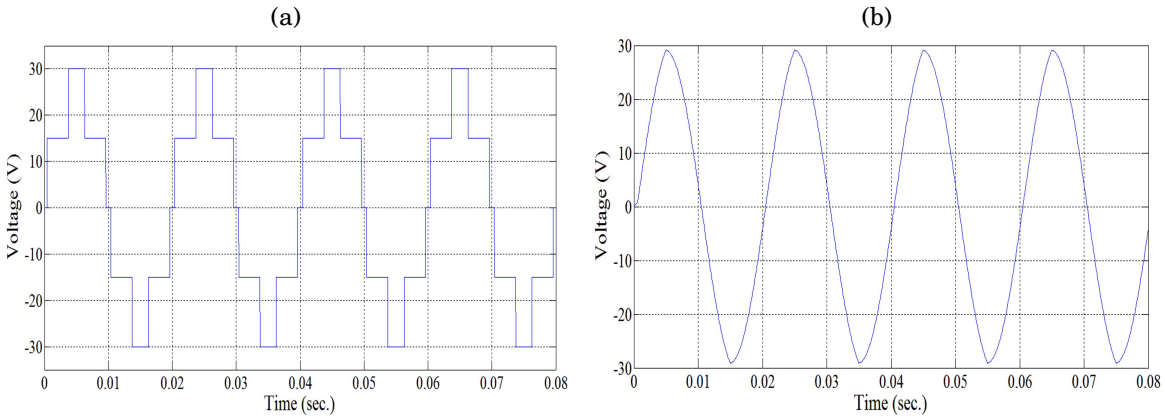

FIGURE 4.20. Simulated output voltages and the corresponding FFT of 5-level inverter without LC filter (left) and with LC filter (right)

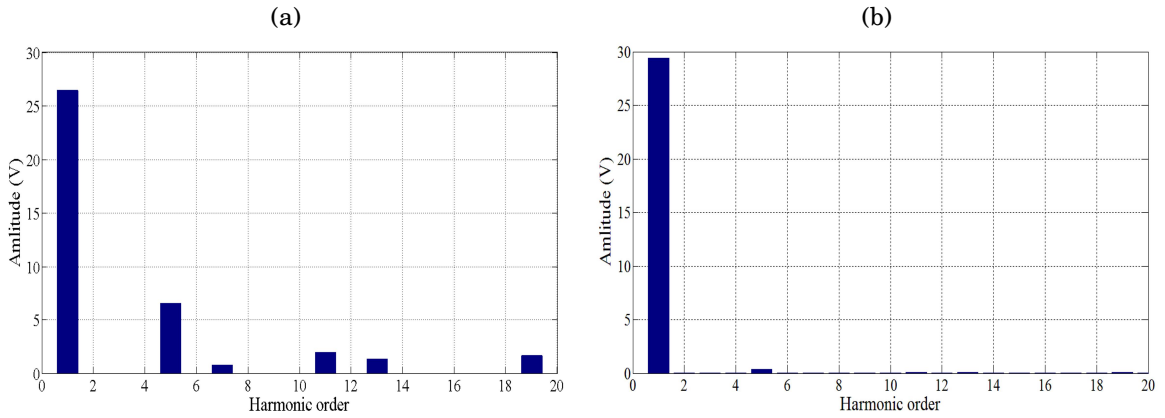

FIGURE 4.21. Simulated output voltages and the corresponding FFT of 5-level inverter without LC filter (left) and with LC filter (right)

Figures 4.20, 4.21, 4.22 and 4.23 show respectively simulated and experimental output voltages generated by the Hybrid Genetic Algorithm based SHE and the corresponding FFT without LC filter (unfiltered output voltage) and with LC filter (filtered output voltage) of 5-level inverter for r = 0.86 (i.e. $\theta_1 = 7.054o$, $\theta_2 = 67.05$) with V_{dc1} = V_{dc2} = 15V.

(a) (b)

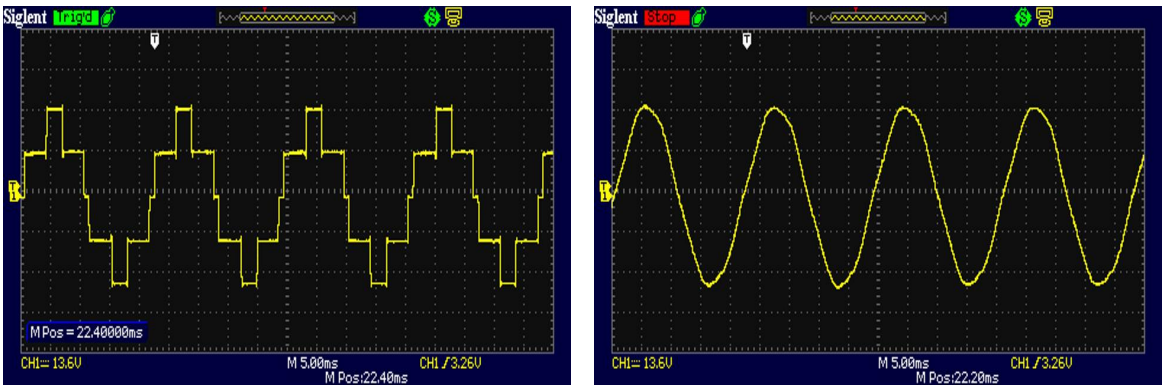

FIGURE 4.22. Experimental output voltages and the corresponding FFT of 5-level inverter without LC filter (left) and with LC filter (right)

(a) (b)

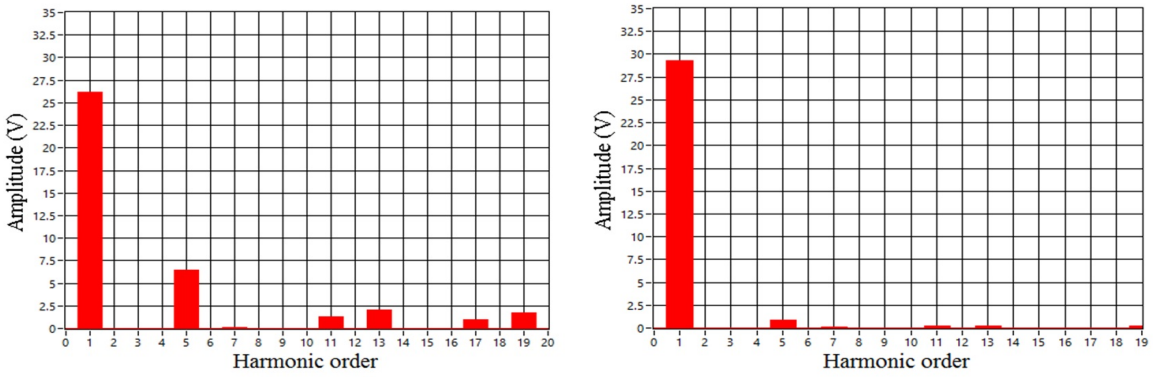

FIGURE 4.23. Experimental output voltages and the corresponding FFT of 5-level inverter without LC filter (left) and with LC filter (right)

4.2.3 Seven level configuration

the7-level configuration is obtained by using the asymmetrical configuration by setting $V_{dc2} = 2V_{dc1}$. The voltage levels for this configuration are generated using table 4.2.

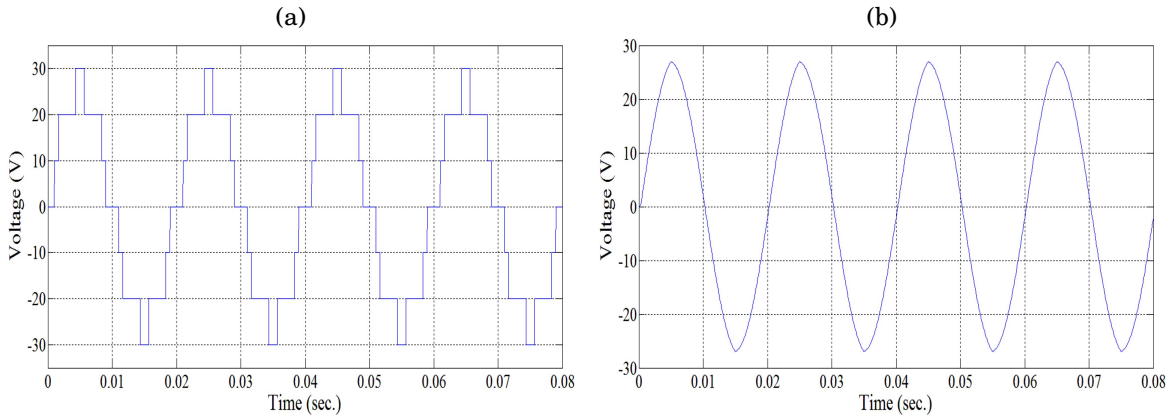

FIGURE 4.24. Simulated output voltages and the corresponding FFT of 7-level inverter without LC filter (left) and with LC filter (right)

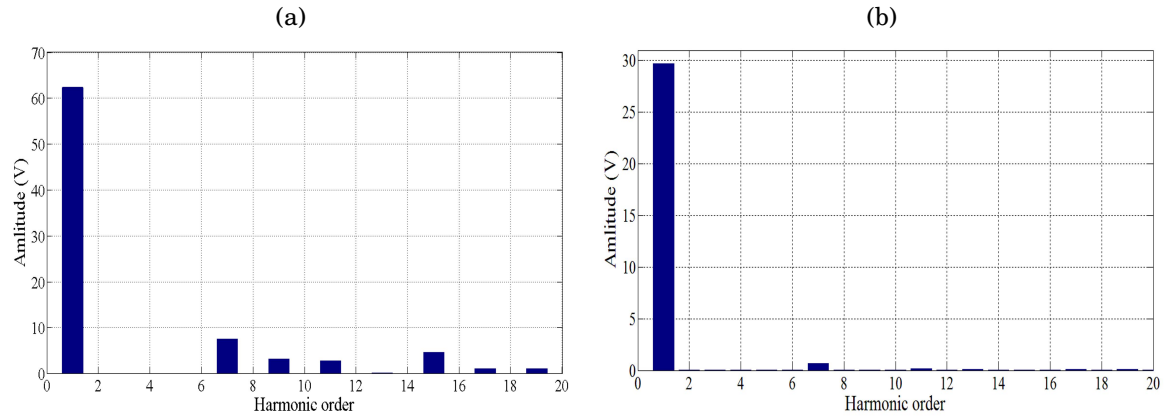

FIGURE 4.25. Simulated output voltages and the corresponding FFT of 7-level inverter without LC filter (left) and with LC filter (right)

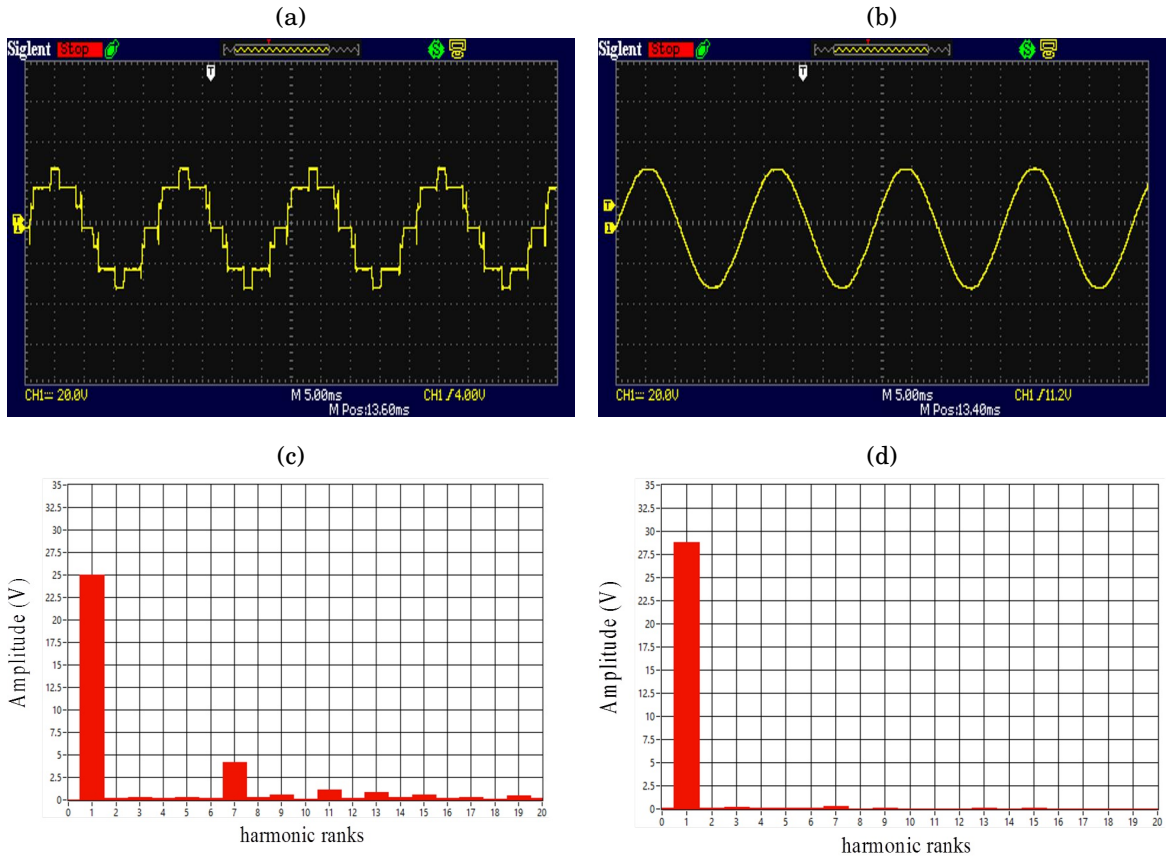

FIGURE 4.26. Experimental output voltages and the corresponding FFT of 7-level inverter without LC filter (left) and with LC filter (right)

4.3 Proposed topology

4.3.1 Topology analysis

The proposed hybrid topology aims to generate high quality AC waveform without using passive filters in order to avoid any loss in power. This can be achieved by using by using non-equal DC input sources (also called asymmetric topology) and using a hybrid configurations of simple H-bridge topology and bidirectional switches in order to generate higher voltage levels with fewer switching devices than conventional topologies. Figure 4.27 shows the structure of the proposed hybrid inverter.

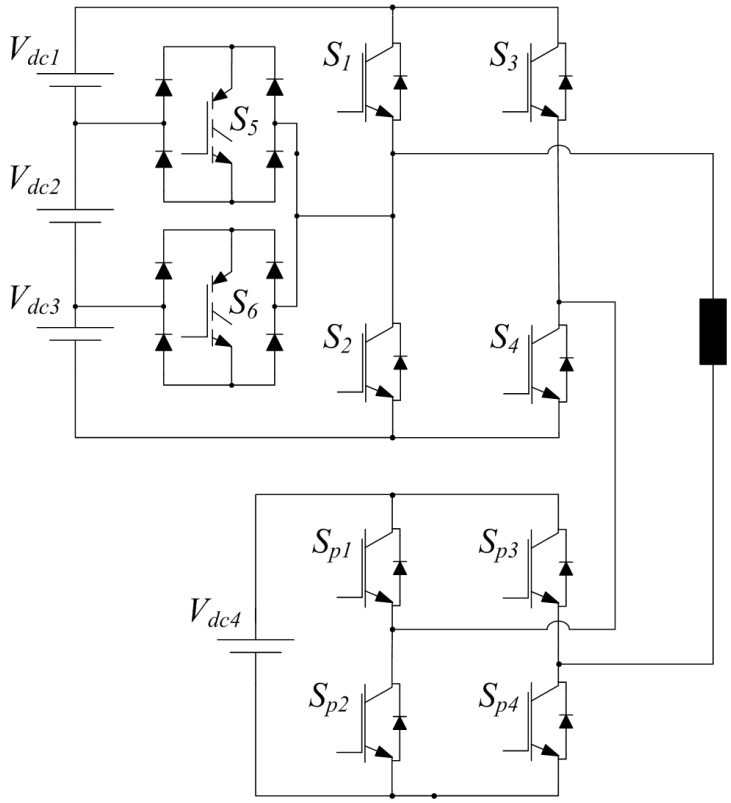

FIGURE 4.27. the proposed hybrid inverter topology.

The converter can be configured in multiple arrangements to generate several voltage levels. This can be done by changing the values of the input DC voltages table 4.4 shows the possible voltage levels that can be generated by the converter. The converter can generate up to twenty-one voltage levels.

Table 4.4: Possible voltages that can be generated by the proposed hybrid inverter.

$V_{dc1}, V_{dc2}, V_{dc3}$	V_{dc4}	m
1	1	9
3	2	11
2	3	13
2	4	15
3	5	17
2	6	19
2	7	21

Figures 4.28, 4.28 and 4.30 show examples of possible voltage combinations, it can be

clearly seen that by increasing the voltage of the fourth DC voltage source (V_{dc4}), the less we have redundant states, which increases the number of voltage levels that can be generated.

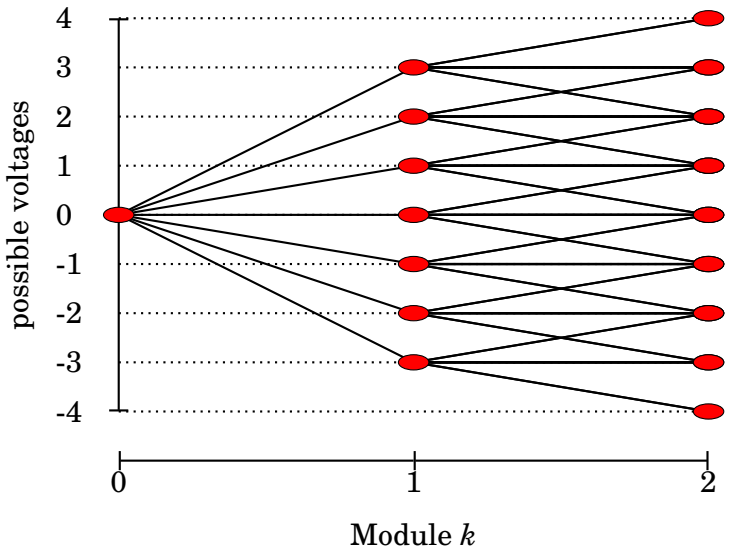

FIGURE 4.28. Possible voltage levels with V_{dc1}=1 , V_{dc2}=3.

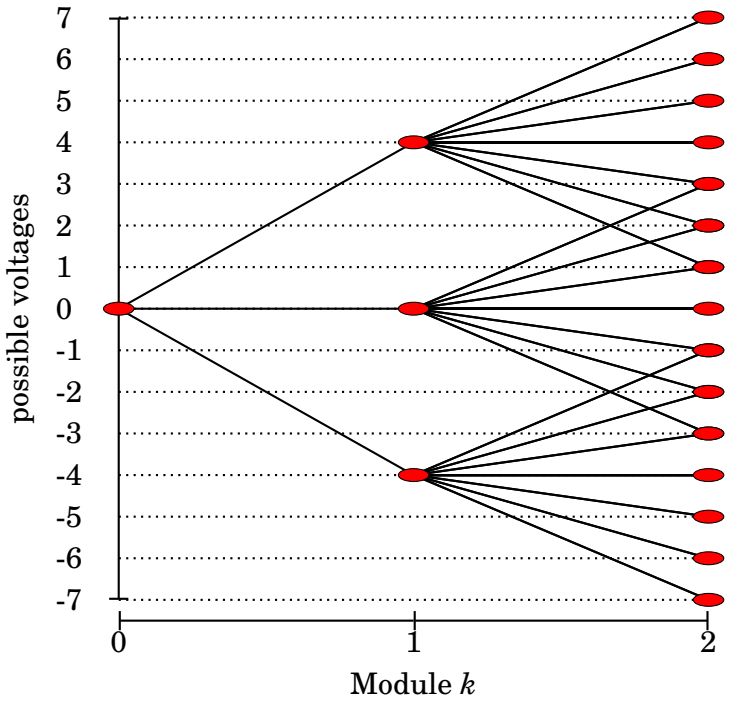

FIGURE 4.29. Possible voltage levels with V_{dc1}=1 , V_{dc2}=4.

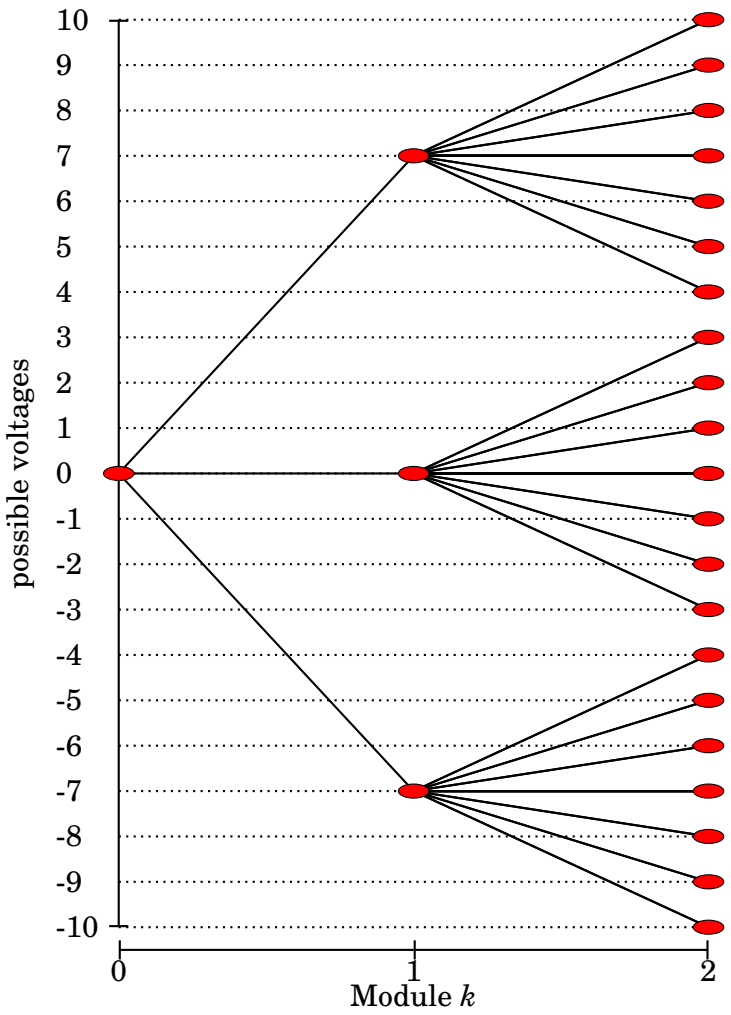

FIGURE 4.30. Possible voltage levels with V_{dc1}=1 , V_{dc2}=7.

When compared to the flying capacitor and clamped diode configurations, the cascade H-bridge multilevel configurations offers a lot of advantages; however, the cascade configurations exhibits an important limitation for higher number of voltage levels. It requires a large number of switching devices, protection circuits, and heatsinks, thereby increasing production cost.

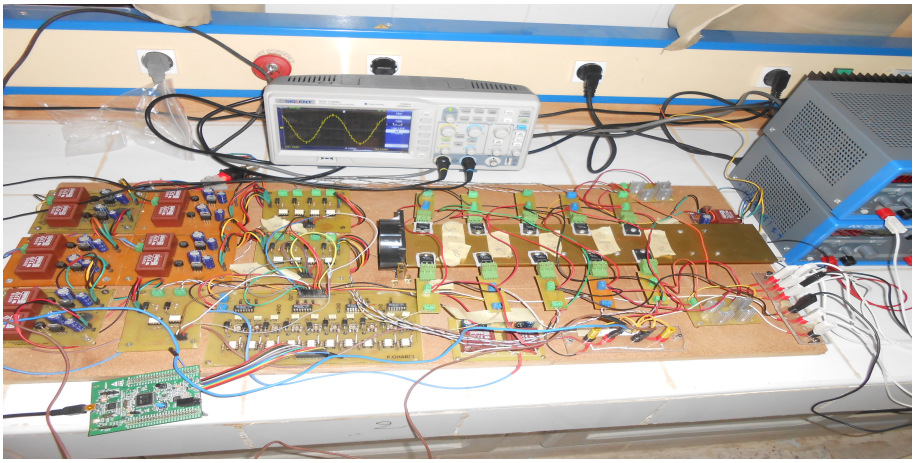

FIGURE 4.31. Experimental setup of the proposed inverter.

The proposed hybrid single phase inverter is composed of two cells connected in series, the upper cell comprises a simple H-bridge formed by S_1, S_2, S_3, S_4 and two bidirectional switches S_5, S_6 and three DC sources with equal voltage values. The function of the bidirectional switches S_5 and S_6 is controlling the connection of the DC sources to construct the desired staircase output voltage waveform. The lower cell is a simple H-bridge formed by S_{p1}, S_{p2}, S_{p3} and S_{p4}, connected to an isolated DC source. The valid switching states for all possible combinations (for twenty-one voltage levels) are presented in Table 4.5, it should be noted that these combinations are only valid for the following conditions:

$$V_{dc1} = V_{dc2} = V_{dc3} \tag{4.4}$$

$$V_{dc4} = 7 \times V_{dc1} \tag{4.5}$$

It means the voltage source connected to the second cell has to be seven times greater than a single voltage source used in the first cell in order to obtain twenty-one voltage levels. It can be seen from Figure 4.27 and equation (4.5) that the switching devices S_{p1}, S_{p2}, S_{p3} and S_{p4} are under higher voltage stress comparing to the switching devices used in the upper bridge, therefore switching devices with high voltage rating must be used in the lower bridge.

Table 4.5: Output voltage levels ($p.u.$) with corresponding conducting switches for the proposed 21-level inverter.

Voltage ($p.u.$)	**Switches in (ON) state**	**Voltage ($p.u.$)**	**Switches in (ON) state**
10	S_1,S_4,S_{p1},S_{p4}	-1	S_3,S_5,S_{p2},S_{p4}
9	S_4,S_5,S_{p1},S_{p4}	-2	S_3,S_6,S_{p2},S_{p4}
8	S_4,S_6,S_{p1},S_{p4}	-3	S_2,S_3,S_{p2},S_{p4}
7	S_2,S_4,S_{p1},S_{p4}	-4	S_1,S_4,S_{p2},S_{p4}
6	S_3,S_5,S_{p1},S_{p4}	-5	S_4,S_5,S_{p2},S_{p4}
5	S_3,S_6,S_{p1},S_{p4}	-6	S_4,S_6,S_{p2},S_{p4}
4	S_2,S_3,S_{p1},S_{p4}	-7	S_2,S_4,S_{p2},S_{p4}
3	S_1,S_4,S_{p2},S_{p4}	-8	S_3,S_5,S_{p2},S_{p4}
2	S_4,S_5,S_{p2},S_{p4}	-9	S_3,S_6,S_{p2},S_{p4}
1	S_4,S_6,S_{p2},S_{p4}	-10	S_2,S_3,S_{p2},S_{p4}
0	S_2,S_4,S_{p2},S_{p4}		

4.3.2 Simulation and experimental results

A small scale laboratory prototype of a single phase 21-level inverter is built in order to verify the analytical and simulation results. H15NA50 (500V, 15A) NPN MOSFETs were used as the switching devices for $S_1,S_2,S_3,S_4,S_{p1},S_{p2},S_{p3}$ and S_{p4} . IRG4PH30K (1200V, 10A) IGBT were used as used as the bidirectional switchesS_5 andS_6. RHRP1560 (600V, 15A) fast switching diodes were used for the bidirectional switches.

The laboratory prototype is shown in Figure 4.31. The control board consists of a STM32F407 microcontroller, the board is used to generate control signals. The gate driver board is built using TLP250 Photocouplers in order to provide electrical isolation between the control board and power circuits and also to provide proper and conditioned gating signals to the MOSFETs. SDS1000 oscilloscope 100MHz 500MS/s was used to capture voltage waveforms.

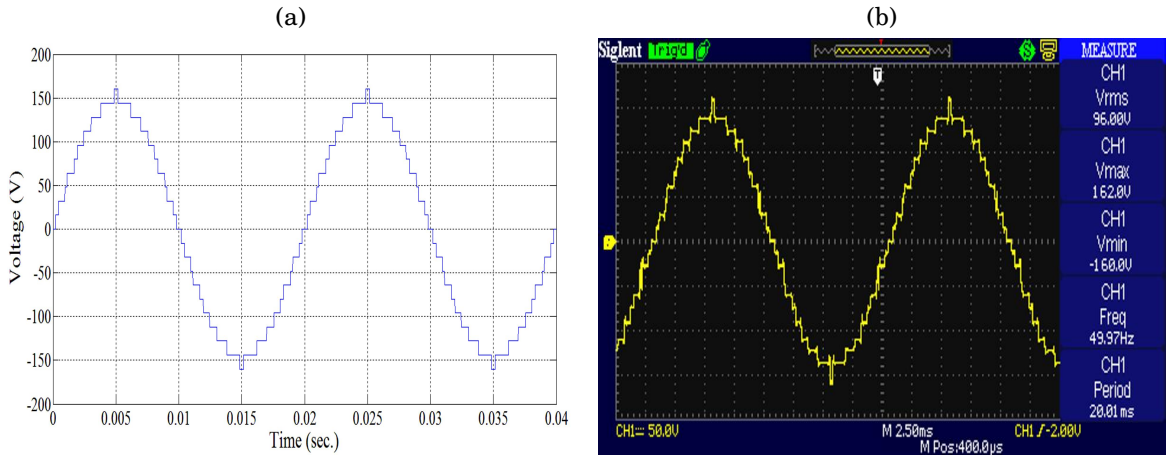

FIGURE 4.32. Voltage waveform generated by the proposed multilevel inverter (simulation and experimental)

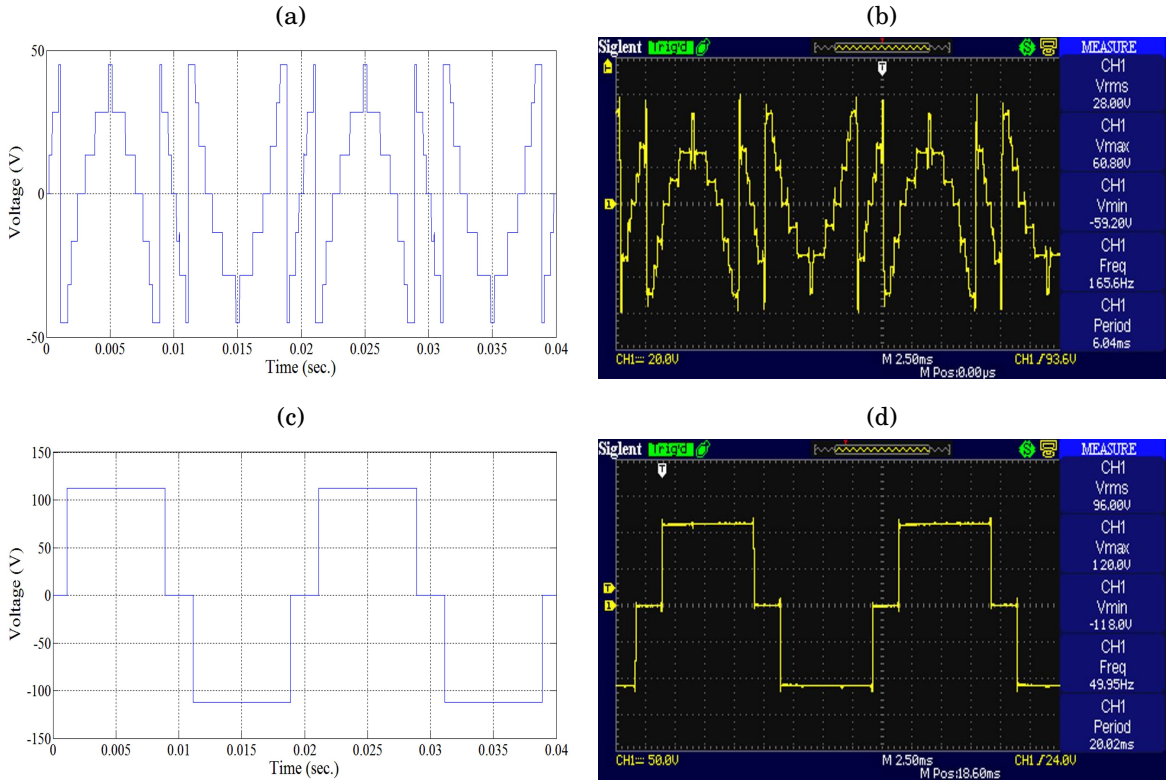

FIGURE 4.33. Voltage waveform generated by the upper cell(simulation(a) experimental(b)) and the lower cell (simulation(c) experimental(d))

Figure 4.32 shows simulated and experimental of twenty-one voltage waveform

pattern, it can be seen from the figures that the simulated pattern matches perfectly experimental result.

Figure 4.33 shows the voltage waveforms generated by the upper and the lower cells. It can be seen from the figure that the first cell is responsible for generating seven voltage levels, whereas the second cell is responsible of generating three voltage levels. It should be noted that the generated voltage patterns stay the same for any modulation index.

Figure 4.34 presents the optimal switching angles (in degrees) found by genetic algorithms, particle swarm optimization, and the HS versus modulation index r with $r \in [0.4, 1.4]$; these angles are computed with a step size of 0.001. It can be seen clearly that the some switching angles by genetic algorithms exceeded the upper limit of the constraint expressed in equation (2.9) for $r \in [0.4, 0.75]$, whereas the HS algorithm was able to generate solutions for all values of r within the desired range. It can be also seen that the particle swarm optimization was not able to generate solutions, particularly at angle θ_1 for $r \in [0.45, 0.5]$ and also $r \in [0.65, 0.7]$, whereas the HS was able to find all angles. The values of the HS algorithm parameters used in this simulation are as follows:$NI = 1000, HMS = 200, HMCR = 0.95$ and $PAR = 0.1$..

Figure 4.35 shows the optimal switching angles (in degrees) generated by the trained ANNs versus modulation index r; the angles are generated with a fine step size of10^{-5}.

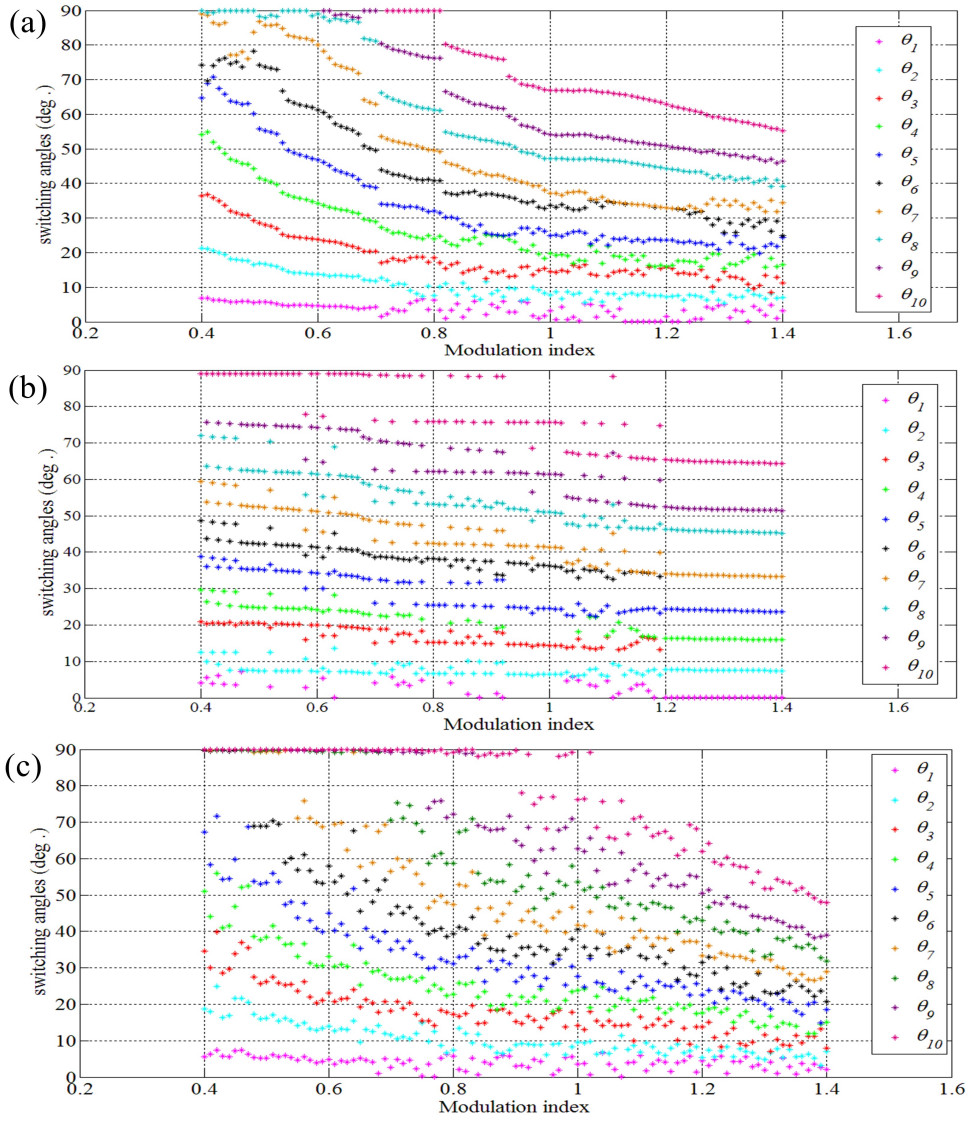

FIGURE 4.34. Switching angles versus modulation index generated by optimization algorithms: (a) genetic algorithm; (b) particle swarm optimization; (c) harmony search

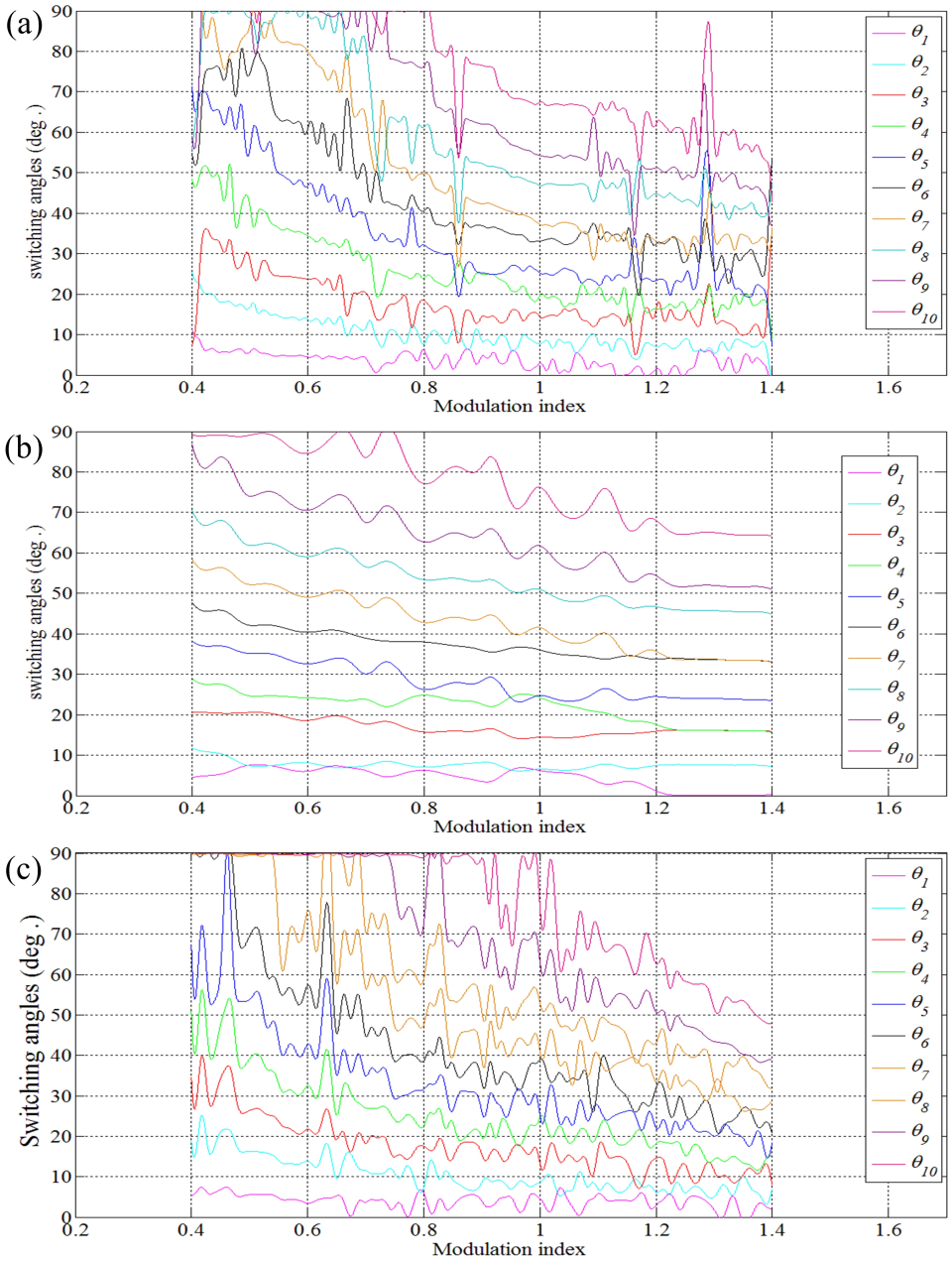

FIGURE 4.35. Switching angles versus modulation index generated using artificial neural networks and trained by: (a) genetic algorithm; (b) particle swarm optimization; (c) harmony search

Figure 4.36 shows the output voltage waveforms generated by the inverter using ANNs trained by different methods for the same modulation index $r = 0.975$. The spectra of the output voltage of the corresponding voltage waveforms are shown in Figure 4.37

and it can be seen from the results that the ANN-HS method was capable of eliminating all the targeted harmonics (from the 3^{rd} to 19^{th}), whereas the other methods were not capable of eliminating all harmonics, as can be seen from the results that the 3^{rd}, 5^{th}, and the 7^{th} harmonics.

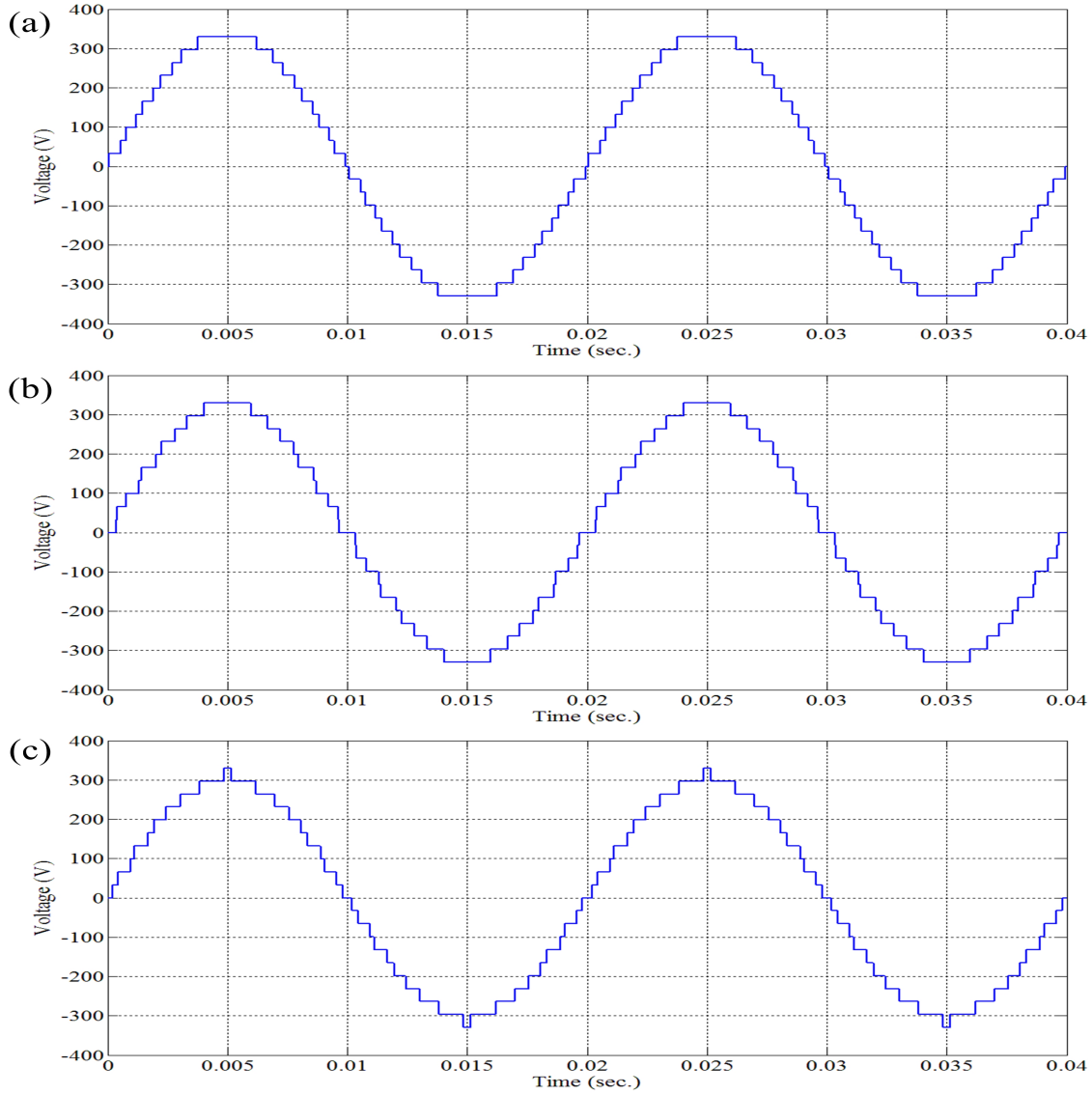

FIGURE 4.36. Voltage waveform generated by the proposed inverter: (a) genetic algorithm; (b) particle swarm optimization; (c) harmony search. (simulation results)

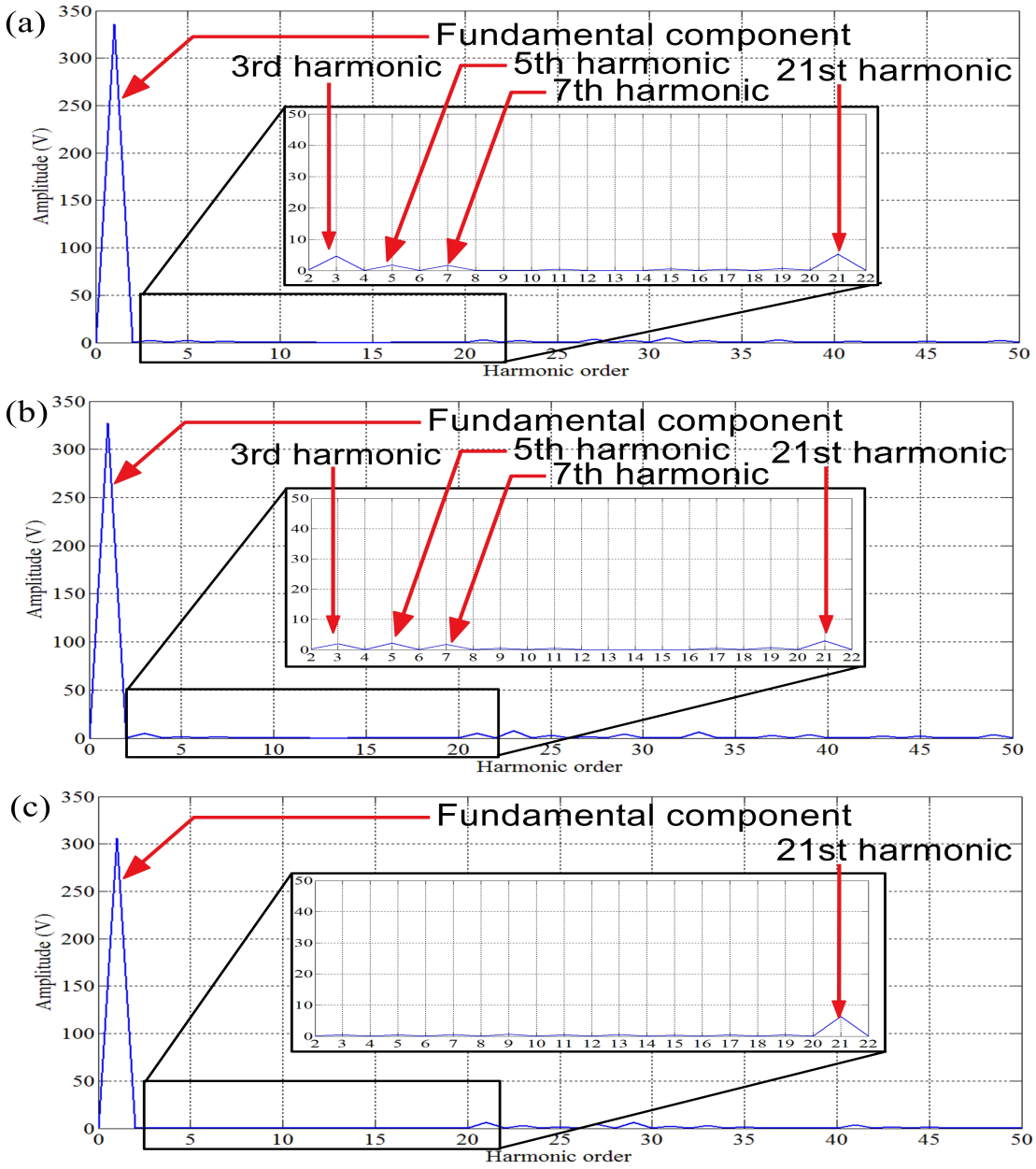

FIGURE 4.37. Fast Fourier transform analysis of the generated voltage waveforms with a modulation index of 0.975: (a) genetic algorithm; (b) particle swarm optimization; (c) harmony search. (simulation results)

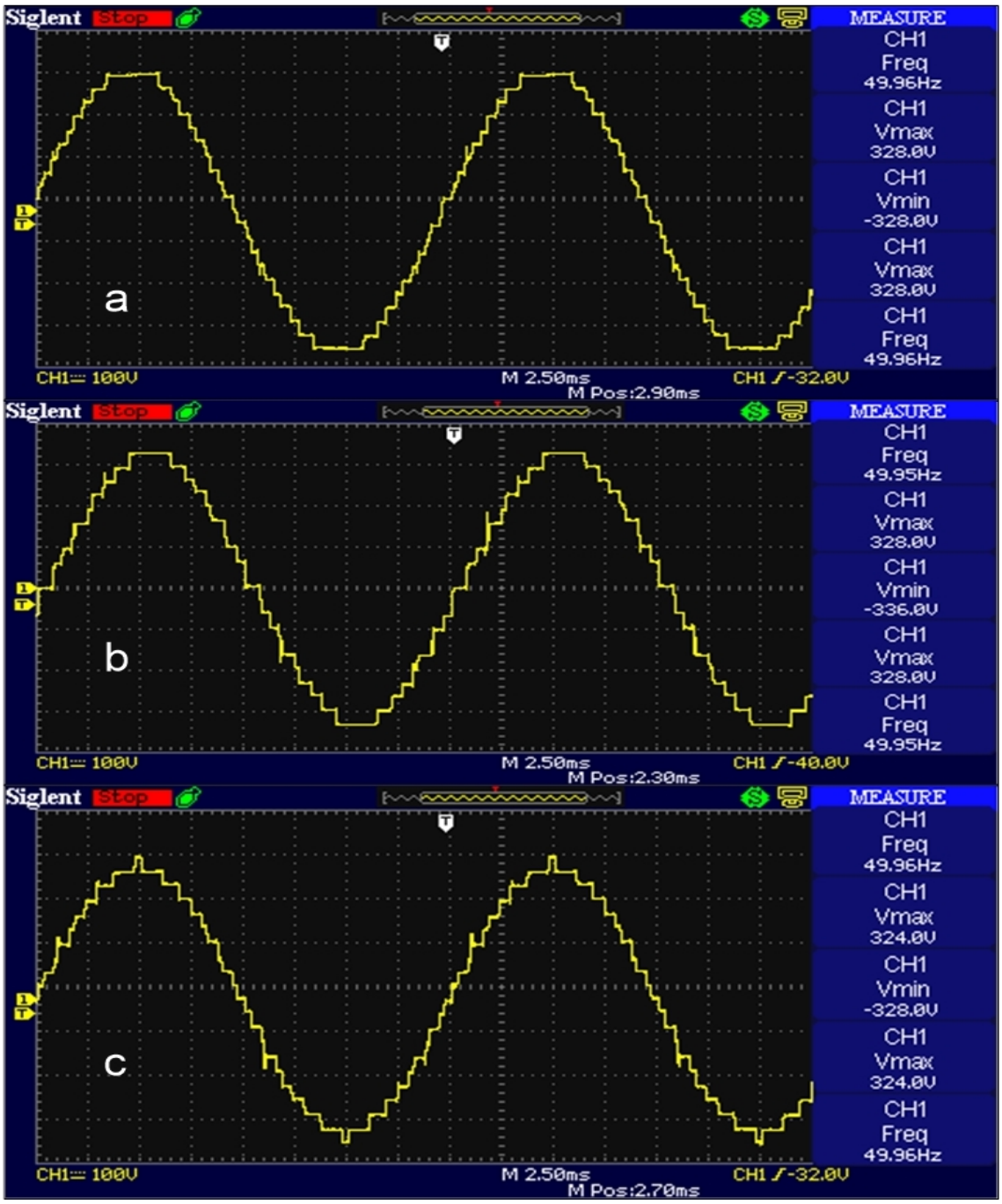

FIGURE 4.38. Voltage waveform generated by the proposed inverter: (a) genetic algorithm; (b) particle swarm optimization; (c) harmony search. (experimental results)

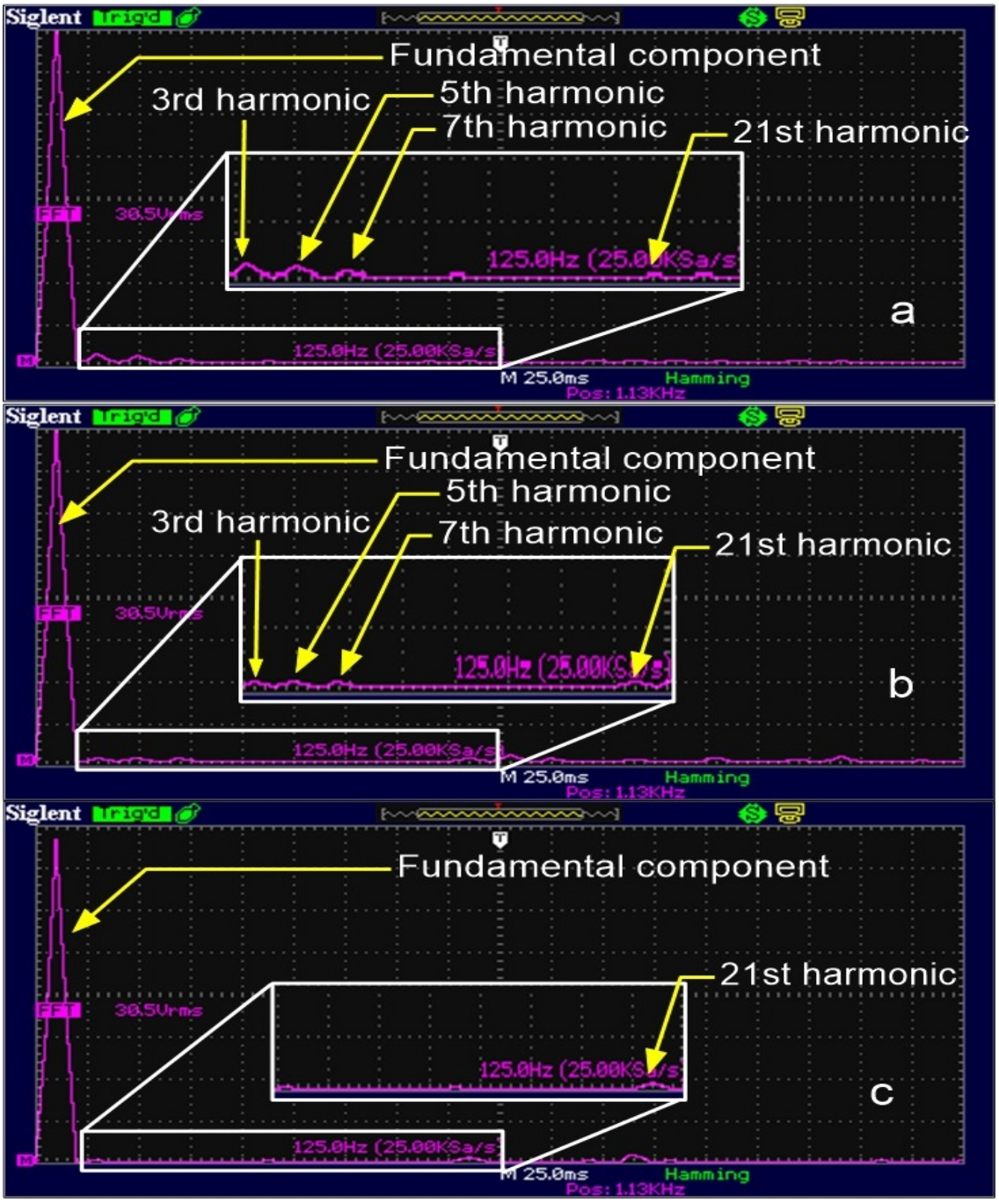

FIGURE 4.39. Fast Fourier transform analysis of the generated voltage waveforms with a modulation index of 0.975: (a) genetic algorithm; (b) particle swarm optimization; (c) harmony search. (experimental results)

4.4 Conclusions

This chapter is divided into three main parts, in first part the selective harmonic elimination strategy was applied to conventional cascaded H-bridge converter; the strategy was tested on the five, seven and nine level configuration in order to see the effect of increasing the number of voltage levels on the quality of the generated waveforms. The strategy also was applied on a three phase seven level converter in order to see its effect on a three phase system. In the second part of this chapter a passive filter was added to the converter, combining the SHEPWM strategy with the ability of the LC filter of filtering high order harmonics resulted in much better harmonic performance than the previous part. Although the great results obtained by combining LC filters with SHEPWM strategy, this method is not suitable for high voltage high power applications due to the nature of the passive filters. In order generate high voltage waveform with minimal power loss, a filterless power converter is needed. The third part of this chapter introduces the proposed multilevel converter, which is a hybrid asymmetric multilevel inverter that can generate up to twenty-one voltage levels, combining this advantage with the selective harmonic elimination strategy resulted in better harmonic performance than the previous configuration.

CONCLUSIONS

A new hybrid asymmetric multilevel inverter with reduced device count is presented was presented, the main advantage of the proposed topology is the high number of voltage levels generated with less switching elements compared to conventional converters. This topology promises a considerable improvement in terms of voltage waveform quality, cost and efficiency.

A real-time harmony search based selective harmonic elimination modulation technique was applied to the proposed inverter topology with the objective of improving performance and extending its life span. The real-time modulation technique is based on artificial neural networks trained using off-line solutions found by harmony search optimization algorithm. In order to validate the theoretical assumptions and simulation results, a small scale prototype of the proposed topology is built, the prototype was a subject to extensive testing. In order to evaluate the performance of the proposed control technique, it was compared to two of the most used optimization algorithms in engineering (genetic algorithm and particle swarm optimization).

The real-time harmony search SHE-PWM has been successfully applied. The method was able to eliminate all the targeted low order harmonics, and performed better than other methods.

The thesis also investigates the possibility of using passive filters along with the selective harmonic elimination modulation strategy. The purpose of using the filters is eliminating high order harmonics. By combining the two techniques, the inverter can generate a high quality voltage waveform with low number of switching devices and switching frequency.However using this approach will lead to a slight loss in power. Using a filterless

multilevel asymmetric inverter will result in better performance in terms of AC voltage quality and energy efficiency. Future work will be focused on exploring new multilevel inverter topologies with reduced device count that can generate a greater number of voltage levels and study the impact of other optimization methods on drive systems.

CHAPTER 5

APPENDIX A

5.1 Schematics

5.1.1 Optocoupler power supplies

The purpose of this circuit is to provide voltage to the gate driver integrated circuits (ICs), the circuit is based on 7815 voltage regulator IC. Figure 5.1 shows a 7815 based power supply for a half bridge circuit.

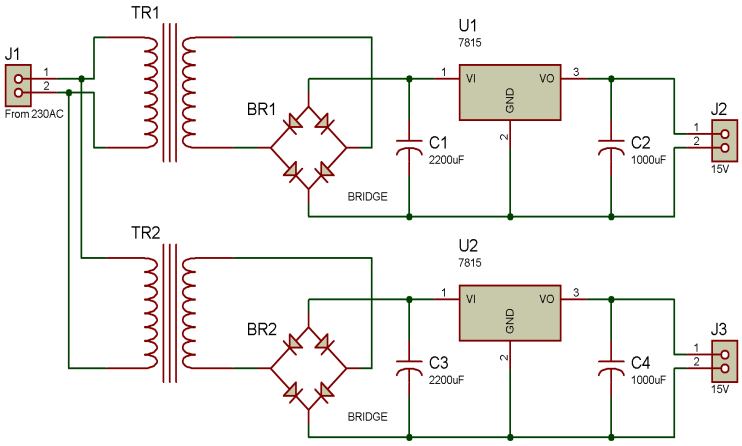

FIGURE 5.1. Optocoupler power supplies

Table 5.1: List of components used in the optocoupler power supplies.

Component index	Value
C1/C3	2200 μf
C2/C4	1000 μf
TR1/TR2	myrra 44087 (primary: 230V 50/60Hz, Secondary: 12V 1.5VA)
U1/U2	7815

5.1.2 Driver board

Figure 5.2 the driver board circuit used in the experiments, the circuit uses the TLP25 IC driver/optocoupler to drive the switching elements. the circuit can drive four IGBTs independently. Table 5.2 shows the list of components used in the driver board circuit

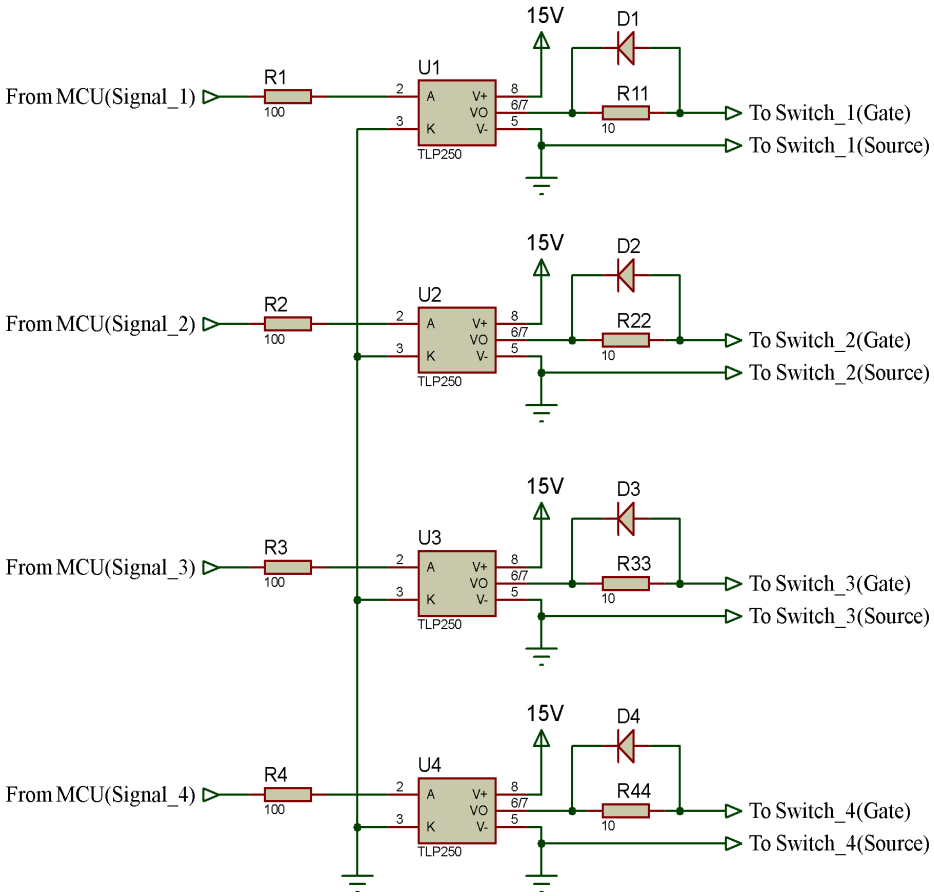

FIGURE 5.2. Driver board circuit

Table 5.2: List of components used in the driver board circuit.

Component index	Value
R1/R2/R3/R4	100 Ω
R11/R22/R33/R44	10 Ω
U1/U2/U3/U4	TLP250
D1/D2/D3/D4	MR856

5.1.3 H-bridge

Figure 5.3 shows the schematic for an H-bridge module. The H-bridge used in some of the experiments is based on H15NA50 power MOSFET with built-in freewheeling diode.

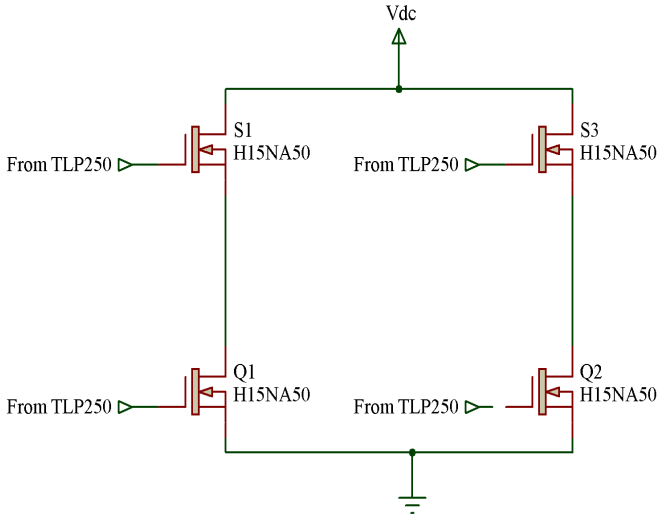

FIGURE 5.3. H-bridge circuit

5.1.4 Bidirectional switch

The bidirectional switch used in the experiments is composed of an IGBT (IRG4PH30K) with four fast switching diode (RHRP156) as figure 5.4 shows.

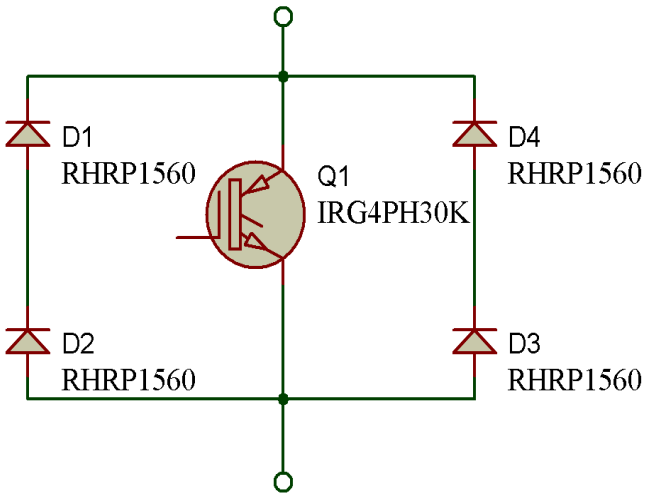

FIGURE 5.4. Bidirectional switch

BIBLIOGRAPHY

[1] J. Lyu, X. Cai, and M. Molinas, "Optimal design of controller parameters for improving the stability of mmc-hvdc for wind farm integration," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, pp. 40–53, March 2018.

[2] X. Zeng, D. Gong, M. Wei, and J. Xie, "Research on novel hybrid multilevel inverter with cascaded h-bridges at alternating current side for high-voltage direct current transmission," *IET Power Electronics*, vol. 11, no. 12, pp. 1914–1925, 2018.

[3] C. A. Rojas, S. Kouro, M. A. Perez, and J. Echeverria, "Dc dc mmc for hvdc grid interface of utility-scale photovoltaic conversion systems," *IEEE Transactions on Industrial Electronics*, vol. 65, pp. 352–362, Jan 2018.

[4] F. L. Luo and H. Ye, "Power electronics: advanced conversion technologies," CRC Press, 2018.

[5] J. Dixon, J. Pereda, C. Castillo, and S. Bosch, "Asymmetrical multilevel inverter for traction drives using only one dc supply," *IEEE Transactions on Vehicular Technology*, vol. 59, pp. 3736–3743, Oct 2010.

[6] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped pwm inverter," *IEEE Transactions on Industry Applications*, vol. IA-17, pp. 518–523, Sept 1981.

[7] K. Wang, Z. Zheng, Y. Li, K. Liu, and J. Shang, "Neutral-point potential balancing of a five-level active neutral-point-clamped inverter," *IEEE Transactions on Industrial Electronics*, vol. 60, pp. 1907–1918, May 2013.

[8] Y. Jiao, F. C. Lee, and S. Lu, "Space vector modulation for 3-level npc converter with neutral voltage balancing and switching loss/noise reduction," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, pp. 1780–1787, March 2014.

[9] L. Zhang, K. Sun, M. Gu, D. Xu, and Y. Gu, "A capacitor voltage balancing control method for five-level full-bridge grid-tied inverters without split-capacitor voltage sampling," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, pp. 2042–2052, Dec 2018.

[10] M. Szarek, A. Penczek, R. Stala, S. Pirog, and A. Mondzik, "Npc three level inverter with dual dc bus for independent distributed generators. neutral-point voltage balancing under the input power imbalance," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, pp. P.1–P.10, Sept 2017.

[11] M. Steczek, A. Chatterjee, and D. Chatterjee, "Optimisation of current harmonics for three-level vsi based induction motor drive suitable for traction application," *IET Power Electronics*, vol. 11, no. 9, pp. 1529–1536, 2018.

[12] A. Tripathi and G. Narayanan, "Torque ripple minimization in neutral-point-clamped three-level inverter fed induction motor drives operated at low-switching-frequency," *IEEE Transactions on Industry Applications*, vol. 54, pp. 2370–2380, May 2018.

[13] M. Hlaili, H. Mechergui, H. Gonçalves, B. Exposto, and J. L. Afonso, "Single phase npc inverter controller with integrated mppt for pv grid connection," in *2016 17th International Conference on Sciences and Techniques of Automatic Control and Computer Engineering (STA)*, pp. 598–605, Dec 2016.

[14] K. Benamrane, T. Abdelkrim, A. Borni, T. Benslimane, and O. Abdelkhalek, "Comparison study of two cascaded configurations of pv generators-three levels inverter for a stand-alone application in south algeria," in *2016 4th International Conference on Control Engineering Information Technology (CEIT)*, pp. 1–6, Dec 2016.

[15] F. Sebaaly, H. Vahedi, H. Y. Kanaan, N. Moubayed, and K. A. Haddad, "Sliding mode fixed frequency current controller design for grid connected npc inverter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, pp. 1397–1405, Dec 2016.

[16] F. Sebaaly, H. Vahedi, H. Y. Kanaan, N. Moubayed, and K. A. Haddad, "Design and implementation of space vector modulation-based sliding mode control for grid-connected 3l npc inverter," *IEEE Transactions on Industrial Electronics*, vol. 63, pp. 7854–7863, Dec 2016.

[17] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE*, pp. 397–403 vol.1, Jun 1992.

[18] K. Antoniewicz, M. Jasinski, M. P. Kazmierkowski, and M. Malinowski, "Model predictive control for three-level four-leg flying capacitor converter operating as shunt active power filter," *IEEE Transactions on Industrial Electronics*, vol. 63, pp. 5255–5262, Aug 2016.

[19] H. B. Richard and H. B. Lawrence, "Electric power converter," Feb. 18 1975. US Patent 3,867,643.

[20] Z. Du, B. Ozpineci, L. M. Tolbert, and J. N. Chiasson, "Dc-ac cascaded h-bridge multilevel boost inverter with no inductors for electric/hybrid electric vehicle applications," *IEEE Transactions on Industry Applications*, vol. 45, pp. 963–970, May 2009.

[21] S. Khomfoi, N. Praisuwanna, and L. M. Tolbert, "A hybrid cascaded multilevel inverter application for renewable energy resources including a reconfiguration technique," in *2010 IEEE Energy Conversion Congress and Exposition*, pp. 3998–4005, Sept 2010.

[22] B. L. Dokić and B. Blanuša, "Power electronics," 2015.

[23] G. Ceglia, V. Guzman, C. Sanchez, F. Ibanez, J. Walter, and M. I. Gimenez, "A new simplified multilevel inverter topology for dc-ac conversion," *IEEE Transactions on Power Electronics*, vol. 21, pp. 1311–1319, Sept 2006.

[24] G.-J. Su, "Multilevel dc-link inverter," *IEEE Transactions on Industry Applications*, vol. 41, pp. 848–854, May 2005.

[25] Y. Hinago and H. Koizumi, "A single phase multilevel inverter using switched series/parallel dc voltage sources," in *2009 IEEE Energy Conversion Congress and Exposition*, pp. 1962–1967, Sept 2009.

[26] Y. Hinago and H. Koizumi, "A single-phase multilevel inverter using switched series/parallel dc voltage sources," *IEEE Transactions on Industrial Electronics*, vol. 57, pp. 2643–2650, Aug 2010.

[27] Y. Hinago and H. Koizumi, "A switched-capacitor inverter using series/parallel conversion with inductive load," *IEEE Transactions on Industrial Electronics*, vol. 59, pp. 878–887, Feb 2012.

[28] S. Du, A. Dekka, B. Wu, and N. Zargari, "Review of high‚Äêpower converters," in *Modular Multilevel Converters: Analysis, Control, and Applications*, IEEE, 2018.

[29] S. Kim, J. Lee, and K. Lee, "A modified level-shifted pwm strategy for fault-tolerant cascaded multilevel inverters with improved power distribution," *IEEE Transactions on Industrial Electronics*, vol. 63, pp. 7264–7274, Nov 2016.

[30] B. Wu, "Cascaded hbridge multilevel inverters," in *High-Power Converters and AC Drives*, IEEE, 2006.

[31] H. Wang, R. Zhao, Y. Deng, and X. He, "Novel carrier-based pwm methods for multilevel inverter," in *IECON-03. 29th Annual Conference of the IEEE Industrial Electronics Society*, vol. 3, pp. 2777–2782, Nov 2003.

[32] G. Konstantinou, R. Darus, J. Pou, S. Ceballos, and V. G. Agelidis, "Varying and unequal carrier frequency pwm techniques for modular multilevel converters," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, pp. 3758–3763, May 2014.

[33] Y. Li, Y. Wang, and B. Q. Li, "Generalized theory of phase-shifted carrier pwm for cascaded h-bridge converters and modular multilevel converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, pp. 589–605, June 2016.

[34] A. K. Sadigh and S. Masoud Barakati, "Topologies and control strategies of multilevel converters," in *Modeling and Control of Sustainable Power Systems: Towards Smarter and Greener Electric Grids* (L. Wang, ed.), pp. 311–340, Berlin, Heidelberg: Springer Berlin Heidelberg, 2012.

[35] A. M. Y. M. Ghias, J. Pou, M. Ciobotaru, and V. G. Agelidis, "Voltage-balancing method using phase-shifted pwm for the flying capacitor multilevel converter," *IEEE Transactions on Power Electronics*, vol. 29, pp. 4521–4531, Sept 2014.

[36] A. M. Y. M. Ghias, J. Pou, G. J. Capella, P. Acuna, and V. G. Agelidis, "On improving phase-shifted pwm for flying capacitor multilevel converters," *IEEE Transactions on Power Electronics*, vol. 31, pp. 5384–5388, Aug 2016.

[37] F. Sasongko, K. Sekiguchi, K. Oguma, M. Hagiwara, and H. Akagi, "Theory and experiment on an optimal carrier frequency of a modular multilevel cascade converter with phase-shifted pwm," *IEEE Transactions on Power Electronics*, vol. 31, pp. 3456–3471, May 2016.

[38] C. D. Townsend, T. J. Summers, and R. E. Betz, "Phase-shifted carrier modulation techniques for cascaded h-bridge multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 62, pp. 6684–6696, Nov 2015.

[39] V. Arun, B. Shanthi, and S. P. Natarajan, "Evaluation of new copwm techniques for three phase seven level diode clamped z-source inverter," in *Recent Advancements in System Modelling Applications* (J. Malathi, R.and Krishnan, ed.), (India), pp. 135–146, Springer India, 2013.

[40] Z. D. Far, A. Radan, and M. D. Far, "Introduction and evaluation of novel multilevel carrier-based pwm strategies using a generalized algorithm," in *2007 European Conference on Power Electronics and Applications*, pp. 1–10, Sept 2007.

[41] V. G. Agelidis and M. Calais, "Application specific harmonic performance evaluation of multicarrier pwm techniques," in *PESC 98 Record. 29th Annual IEEE Power Electronics Specialists Conference (Cat. No.98CH36196)*, vol. 1, pp. 172–178 vol.1, May 1998.

[42] P. M. Meshram and V. B. Borghate, "A simplified nearest level control (nlc) voltage balancing method for modular multilevel converter (mmc)," *IEEE Transactions on Power Electronics*, vol. 30, pp. 450–462, Jan 2015.

[43] J. Wang, H. Ma, and Z. Bai, "A submodule fault ride-through strategy for modular multilevel converters with nearest level modulation," *IEEE Transactions on Power Electronics*, vol. 33, pp. 1597–1608, Feb 2018.

[44] M. Perez, J. Rodriguez, J. Pontt, and S. Kouro, "Power distribution in hybrid multicell converter with nearest level modulation," in *2007 IEEE International Symposium on Industrial Electronics*, pp. 736–741, June 2007.

[45] M. Moranchel, E. J. Bueno, F. J. Rodriguez, and I. Sanz, "Implementation of nearest level modulation for modular multilevel converter," in *2015 IEEE*

6th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), pp. 1–5, June 2015.

[46] C. Hu, G. Holmes, W. Shen, X. Yu, Q. Wang, and F. Luo, "Neutral-point potential balancing control strategy of three-level active npc inverter based on shepwm," *IET Power Electronics*, vol. 10, no. 14, pp. 1943–1950, 2017.

[47] M. Zabaleta, E. Burguete, D. Madariaga, I. Zubimendi, M. Zubiaga, and I. Larrazabal, "Lclgrid filter design of a multimegawatt medium-voltage converter for offshore wind turbine using shepwm modulation," *IEEE Transactions on Power Electronics*, vol. 31, pp. 1993–2001, March 2016.

[48] Z. Zhao, Y. Zhong, H. Gao, L. Yuan, and T. Lu, "Hybrid selective harmonic elimination pwm for common-mode voltage reduction in three-level neutral-point-clamped inverters for variable speed induction drives," *IEEE Transactions on Power Electronics*, vol. 27, pp. 1152–1158, March 2012.

[49] S. S. Lee, B. Chu, N. R. N. Idris, H. H. Goh, and Y. E. Heng, "Switched-battery boost-multilevel inverter with ga optimized shepwm for standalone application," *IEEE Transactions on Industrial Electronics*, vol. 63, pp. 2133–2142, April 2016.

[50] J. Pontt, J. Rodriguez, and R. Huerta, "Mitigation of noneliminated harmonics of shepwm three-level multipulse three-phase active front end converters with low switching frequency for meeting standard ieee 519 92," *IEEE Transactions on Power Electronics*, vol. 19, pp. 1594–1600, Nov 2004.

[51] M. Hajizadeh and S. H. Fathi, "Selective harmonic elimination strategy for cascaded h-bridge five-level inverter with arbitrary power sharing among the cells," *IET Power Electronics*, vol. 9, no. 1, pp. 95–101, 2016.

[52] H. S. Patel and R. G. Hoft, "Generalized techniques of harmonic elimination and voltage control in thyristor inverters: Part ii — voltage control techniques,"

IEEE Transactions on Industry Applications, vol. IA-10, pp. 666–673, Sept 1974.

[53] F. Chabni, R. Taleb, and M. Helaimi, "Optimum shepwm for a new 21-level inverter topology using numerical optimization methods: experimental comparative study," *Journal of Vibration and Control*, 2018.

[54] F. Chabni, R. Taleb, and M. Helaimi, "Output voltage waveform improvement of modified cascaded h-bridge multilevel inverter using selective harmonic elimination technique based on hybrid genetic algorithm," *REVUE ROUMAINE DES SCIENCES TECHNIQUES-SERIE ELECTROTECHNIQUE ET ENERGETIQUE*, vol. 62, no. 4, pp. 405–410, 2017.

[55] M. S. A. Dahidah and V. G. Agelidis, "Selective harmonic elimination pwm control for cascaded multilevel voltage source converters: A generalized formula," *IEEE Transactions on Power Electronics*, vol. 23, pp. 1620–1630, July 2008.

[56] F. Chabni, R. Taleb, and A. Benbouali, "Multiple switching patterns for three-level shepwm inverter using stm32f4 microcontroller," in *2017 5th International Conference on Electrical Engineering - Boumerdes (ICEE-B)*, pp. 1–6, Oct 2017.

[57] T. Jalakas, D. Vinnikov, T. Lehtla, and V. Bolgov, "Interlock delay time minimization and its impact on the high-voltage half-bridge dc/dc converter," in *2009 Compatibility and Power Electronics*, pp. 438–443, May 2009.

[58] H. Zhang, B. Kou, L. Zhang, and H. Zhang, "Analysis and compensation of dead-time effect of a zvt pwm inverter considering the rise- and fall-times," *Applied Sciences*, vol. 6, no. 11, pp. 1–17, 2016.

[59] S.-H. Kim, "Chapter 7 - pulse width modulation inverters," in *Electric Motor Control* (S.-H. Kim, ed.), pp. 265 – 340, Elsevier, 2017.

[60] D. OSullivan and M. Moroney in *Enhancing Industrial Motor Control Performance Utilizing Digital Isolator Technology-MS-2758 technical article*, pp. 1– 6, Analog Devices, Inc., 2014.

[61] L. Ben-Brahim, "On the compensation of dead time and zero-current crossing for a pwm-inverter-controlled ac servo drive," *IEEE Transactions on Industrial Electronics*, vol. 51, pp. 1113–1118, Oct 2004.

[62] M. A. Khanesar, H. Tavakoli, M. Teshnehlab, and M. A. Shoorehdeli, "Novel binary particle swarm optimization," in *Particle Swarm Optimization* (A. Lazinica, ed.), ch. 1, IntechOpen, 2009.

[63] M. B. Abdelhalim and S. E. D. Habib, "Particle swarm optimization for hw/sw partitioning," in *Particle Swarm Optimization* (A. Lazinica, ed.), ch. 3, IntechOpen, 2009.

[64] J. Kennedy and R. Eberhart, "Particle swarm optimization," in *Proceedings of ICNN'95 - International Conference on Neural Networks*, vol. 4, pp. 1942–1948 vol.4, Nov 1995.

[65] R. Eberhart and J. Kennedy, "A new optimizer using particle swarm theory," in *MHS'95. Proceedings of the Sixth International Symposium on Micro Machine and Human Science*, pp. 39–43, Oct 1995.

[66] W. Hu, H. Wang, L. Yan, and B. Du, "A hybrid cellular swarm optimization method for traffic-light scheduling," *Chinese Journal of Electronics*, vol. 27, no. 3, pp. 611–616, 2018.

[67] M. A. Memon, S. Mekhilef, and M. Mubin, "Selective harmonic elimination in multilevel inverter using hybrid apso algorithm," *IET Power Electronics*, vol. 11, no. 10, pp. 1673–1680, 2018.

[68] R. Tavoli and M. Keyvanpour, "A method for handwritten word spotting based on particle swarm optimisation and multi-layer perceptron," *IET Software*, vol. 12, no. 2, pp. 152–159, 2018.

[69] Y. Wang, D. Chang, Y. Fan, G. Zhang, J. Zhan, X. Shao, and W. He, "Acoustic localization of partial discharge sources in power transformers using a particle-swarm-optimization-route-searching algorithm," *IEEE Transactions on Dielectrics and Electrical Insulation*, vol. 24, pp. 3647–3656, Dec 2017.

[70] X. Wang, Z. Yang, and X. Yan, "Novel particle swarm optimization-based variational mode decomposition method for the fault diagnosis of complex rotating machinery," *IEEE/ASME Transactions on Mechatronics*, vol. 23, pp. 68–79, Feb 2018.

[71] T. S. Babu, J. P. Ram, T. Dragi*f*çevi*f*á, M. Miyatake, F. Blaabjerg, and N. Rajasekar, "Particle swarm optimization based solar pv array reconfiguration of the maximum power extraction under partial shading conditions," *IEEE Transactions on Sustainable Energy*, vol. 9, pp. 74–85, Jan 2018.

[72] A. Chipperfield and P. Fleming, "The matlab genetic algorithm toolbox," in *IET Conference Proceedings*, pp. 10(1)–10(4), Institution of Engineering and Technology, January 1995.

[73] J. H. Holland, *Adaptation in natural and artificial systems: an introductory analysis with applications to biology, control, and artificial intelligence*.
MIT press, 1992.

[74] B. Lorenzo and S. Glisic, "Optimal routing and traffic scheduling for multihop cellular networks using genetic algorithm," *IEEE Transactions on Mobile Computing*, vol. 12, pp. 2274–2288, Nov 2013.

[75] K. Prasad, R. Ranjan, N. C. Sahoo, and A. Chaturvedi, "Optimal reconfiguration of radial distribution systems using a fuzzy mutated genetic algorithm," *IEEE Transactions on Power Delivery*, vol. 20, pp. 1211–1213, April 2005.

[76] L. Kawecki and T. Niewierowicz, “Hybrid genetic algorithm to solve the two point boundary value problem in the optimal control of induction motors,” *IEEE Latin America Transactions*, vol. 12, pp. 176–181, March 2014.

[77] E. Israeli and E. Gilad, “Novel genetic algorithm for loading pattern optimization based on core physics heuristics,” *Annals of Nuclear Energy*, vol. 118, pp. 35 – 48, 2018.

[78] A. Senoussi, S. Dauzere-Peres, N. Brahimi, B. Penz, and N. K. Mouss, “Heuristics based on genetic algorithms for the capacitated multi vehicle production distribution problem,” *Computers and Operations Research*, vol. 96, pp. 108 – 119, 2018.

[79] O. Kramer, *Genetic algorithm essentials*, vol. 679.
Springer, 2017.

[80] J. S. Arora, “Chapter 16 - genetic algorithms for optimum design,” in *Introduction to Optimum Design (Third Edition)* (J. S. Arora, ed.), pp. 643 – 655, Boston: Academic Press, third edition ed., 2012.

[81] R. Storn, “On the usage of differential evolution for function optimization,” in *Proceedings of North American Fuzzy Information Processing*, pp. 519–523, June 1996.

[82] R. Storn and K. Price, “Differential evolution ‚Äì a simple and efficient heuristic for global optimization over continuous spaces,” *Journal of Global Optimization*, vol. 11, p. 341‚Äì359, December 1997.

[83] Z. Gao, Z. Pan, and J. Gao, “A new highly efficient differential evolution scheme and its application to waveform inversion,” *IEEE Geoscience and Remote Sensing Letters*, vol. 11, pp. 1702–1706, Oct 2014.

[84] H. K. Diem, V. D. Trung, N. T. Trung, V. V. Tai, and N. T. Thao, "A differential evolution-based clustering for probability density functions," *IEEE Access*, vol. 6, pp. 41325–41336, 2018.

[85] J. Ri, L. Liu, Y. Liu, H. Wu, W. Huang, and H. Kim, "Optimal weighted extreme learning machine for imbalanced learning with differential evolution [research frontier]," *IEEE Computational Intelligence Magazine*, vol. 13, pp. 32–47, Aug 2018.

[86] J. Hu, M. Wu, X. Chen, S. Du, P. Zhang, W. Cao, and J. She, "A multilevel prediction model of carbon efficiency based on the differential evolution algorithm for the iron ore sintering process," *IEEE Transactions on Industrial Electronics*, vol. 65, pp. 8778–8787, Nov 2018.

[87] A. Qing, *Fundamentals of Differential Evolution*.
IEEE, 2009.

[88] L. M. Zheng, S. X. Zhang, K. S. Tang, and S. Y. Zheng, "Differential evolution powered by collective information," *Information Sciences*, vol. 399, pp. 13–29, March 2017.

[89] R. Vijayakumar, C. Devalalitha, A. Nachiappan, and R. Mazhuvendhi, "Selective harmonic elimination pwm method using two level inverter by differential evolution optimization technique," in *2014 International Conference on Science Engineering and Management Research (ICSEMR)*, pp. 1–6, November 2014.

[90] M. I. M. Rashid, A. Hiendro, and M. Anwari, "Optimal he-pwm inverter switching patterns using differential evolution algorithm," in *2012 IEEE International Conference on Power and Energy (PECon)*, pp. 32–37, December 2012.

[91] C. Sun, H. Zhou, and L. Chen, "Improved differential evolution algorithms," in *2012 IEEE International Conference on Computer Science and Automation Engineering (CSAE)*, vol. 3, pp. 142–145, May 2012.

[92] T. Goel and N. Stander, "Adaptive simulated annealing for global optimization in ls-opt," in *7th Euro LS-DYNA Conf Proc*, 2009.

[93] O. K. Erol and I. Eksin, "A new optimization method: big bang–big crunch," *Advances in Engineering Software*, vol. 37, no. 2, pp. 106–111, 2006.

[94] C. K. Panigrahi, P. K. Chattopadhyay, R. N. Chakrabarti, and M. Basu, "Simulated annealing technique for dynamic economic dispatch," *Electric Power Components and Systems*, vol. 34, no. 5, pp. 577–586, 2006.

[95] F. Chabni, R. Taleb, and M. Hatti, "Application of simulated annealing optimization algorithm in selective harmonic elimination problem," in *International Conference in Artificial Intelligence in Renewable Energetic Systems*, pp. 375–382, Springer, 2017.

[96] X. Wang, X.-Z. Gao, and K. Zenger, *An introduction to harmony search optimization method*.
Springer, 2015.

[97] Z. W. Geem, J. H. Kim, and G. Loganathan, "A new heuristic optimization algorithm: Harmony search," *SIMULATION*, vol. 76, no. 2, pp. 60–68, 2001.

[98] Z. Geem, J. Kim, and G. Loganathan, "Harmony search optimization: Application to pipe network design," *International Journal of Modelling and Simulation*, vol. 22, no. 2, pp. 125–133, 2002.

[99] F. Mzoughi, S. Bouallegue, M. Ayadi, A. J. Garrido, and I. Garrido, "Harmony search algorithm-based airflow control of an oscillating water column-based wave generation power plants," in *2018 International Conference on Advanced Systems and Electric Technologies*, pp. 249–254, March 2018.

[100] D. Zou, H. Liu, and L. Gao, "A modified global harmony search algorithm for robust pid controller tuning," in *Proceedings of the 30th Chinese Control Conference*, pp. 2158–2163, July 2011.

[101] M. N. Ambia, H. M. Hasanien, A. Al-Durra, and S. M. Muyeen, "Harmony search algorithm-based controller parameters optimization for a distributed-generation system," *IEEE Transactions on Power Delivery*, vol. 30, pp. 246–255, Feb 2015.

[102] M. B. B. Mahaleh and S. A. Mirroshandel, "Harmony search path detection for vision based automated guided vehicle," *Robotics and Autonomous Systems*, vol. 107, pp. 156–166, September 2018.

[103] H. V. H. Ayala, L. d. S. Coelho, V. C. Mariani, M. V. F. d. Luz, and J. V. Leite, "Harmony search approach based on ricker map for multi-objective transformer design optimization," *IEEE Transactions on Magnetics*, vol. 51, pp. 1–4, March 2015.

[104] Y. Y. Moon, Z. W. Geem, and G.-T. Han, "Vanishing point detection for self-driving car using harmony search algorithm," *Swarm and Evolutionary Computation*, vol. 41, pp. 111–119, August 2018.

[105] D. C. Hoang, P. Yadav, R. Kumar, and S. K. Panda, "Real-time implementation of a harmony search algorithm-based clustering protocol for energy-efficient wireless sensor networks," *IEEE Transactions on Industrial Informatics*, vol. 10, pp. 774–783, Feb 2014.

[106] J. H. Kim, H. M. Lee, and D. G. Yoo, "Investigating the convergence characteristics of harmony search," in *Harmony Search Algorithm*, pp. 3–10, Springer, 2016.

[107] A. Askarzadeh and A. Rezazadeh, "An innovative global harmony search algorithm for parameter identification of a pem fuel cell model," *IEEE Transactions on Industrial Electronics*, vol. 59, pp. 3473–3480, Sept 2012.

[108] D. Graupe, *Principles of artificial neural networks*, vol. 7.
World Scientific, 2013.

[109] C. S. Berger, "Recursive single-layer nets for output error dynamic models," *IEEE Transactions on Neural Networks*, vol. 6, pp. 508–511, March 1995.

[110] S. Bhama and H. Singh, "Single layer neural networks for linear system identification using gradient descent technique," *IEEE Transactions on Neural Networks*, vol. 4, pp. 884–888, Sept 1993.

[111] Y. Hayashi, M. Sakata, and S. I. Gallant, "Multi-layer versus single-layer neural networks and an application to reading hand-stamped characters," in *International Neural Network Conference: July 9-13, 1990 Palais Des Congres, Paris, France*, pp. 781–784, Springer Netherlands, 1990.

[112] A. Addeh, A. Khormali, and N. A. Golilarz, "Control chart pattern recognition using rbf neural network with new training algorithm and practical features," *ISA Transactions*, vol. 79, pp. 202–216, August 2018.

[113] S.-W. Lee and H.-H. Song, "A new recurrent neural-network architecture for visual pattern recognition," *IEEE Transactions on Neural Networks*, vol. 8, pp. 331–340, March 1997.

[114] S. Sieniutycz and Z. Szwast, "4 - neural networks‚Äîa review of applications," in *Optimizing Thermal, Chemical, and Environmental Systems* (S. Sieniutycz and Z. Szwast, eds.), pp. 109–120, Elsevier, 2018.

[115] G. Nowak and A. Rusin, "Using the artificial neural network to control the steam turbine heating process," *Applied Thermal Engineering*, vol. 108, pp. 204–210, September 2016.

[116] F. Rodriguez, A. Fleetwood, A. Galarza, and L. Fontan, "Predicting solar energy generation through artificial neural networks using weather forecasts for microgrid control," *Renewable Energy*, vol. 126, pp. 855–864, October 2018.

[117] P. Brandstetter and M. Kuchar, “Sensorless control of variable speed induction motor drive using rbf neural network,” *Journal of Applied Logic*, vol. 24, pp. 97–108, November 2017.

[118] N. Najmaei and M. R. Kermani, “Applications of artificial intelligence in safe human‚Äìrobot interactions,” *IEEE Transactions on Systems, Man, and Cybernetics, Part B (Cybernetics)*, vol. 41, pp. 448–459, April 2011.

[119] C. McCool, T. Perez, and B. Upcroft, “Mixtures of lightweight deep convolutional neural networks: Applied to agricultural robotics,” *IEEE Robotics and Automation Letters*, vol. 2, pp. 1344–1351, July 2017.

[120] L. Jin, S. Li, J. Yu, and J. He, “Robot manipulator control using neural networks: A survey,” *Neurocomputing*, vol. 285, pp. 23–34, April 2018.

[121] M. I. Jordan and C. M. Bishop, “66 neural networks,” in *Computer science handbook* (A. B. Tucker, ed.), CRC press, 2004.

[122] J. Gomes and V. Barroso, “Unsupervised learning for channel equalization using a neural network data receiver,” in *Proceedings of ICNN’95 - International Conference on Neural Networks*, vol. 1, pp. 502–506, November 1995.